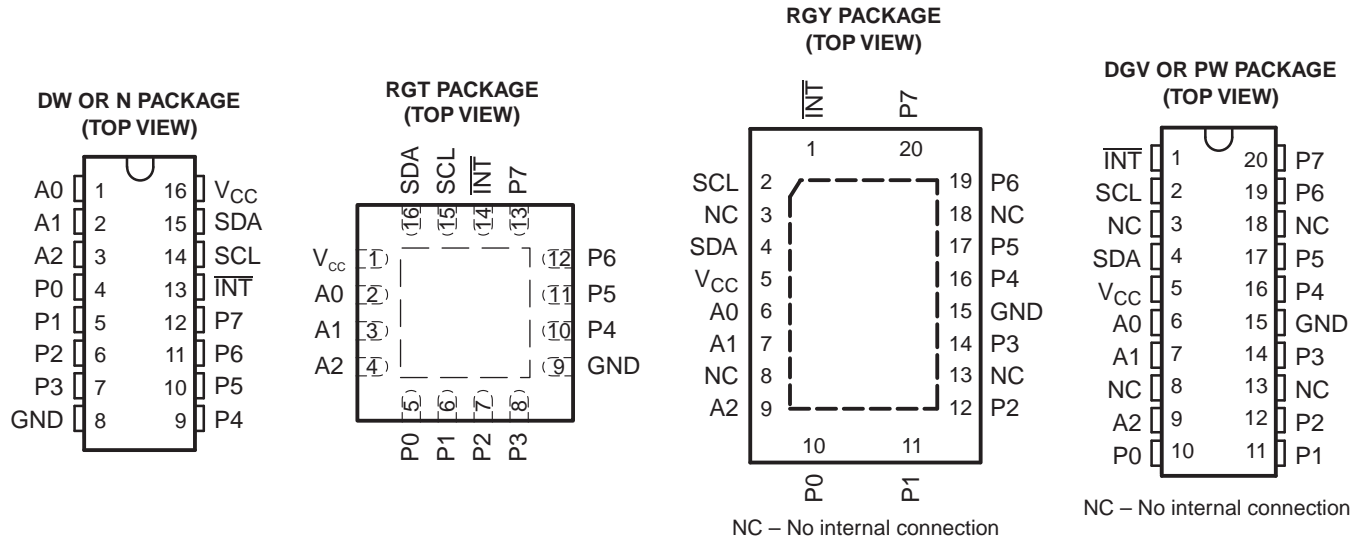


## REMOTE 8-BIT I/O EXPANDER FOR I<sup>2</sup>C BUS

### FEATURES

- Low Standby-Current Consumption of 10  $\mu$ A Max
- I<sup>2</sup>C to Parallel-Port Expander
- Open-Drain Interrupt Output
- Compatible With Most Microcontrollers
- Latched Outputs With High-Current Drive Capability for Directly Driving LEDs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II



### DESCRIPTION/ORDERING INFORMATION

This 8-bit input/output (I/O) expander for the two-line bidirectional bus (I<sup>2</sup>C) is designed for 2.5-V to 6-V V<sub>CC</sub> operation.

The PCF8574 provides general-purpose remote I/O expansion for most microcontroller families via the I<sup>2</sup>C interface [serial clock (SCL), serial data (SDA)].

The device features an 8-bit quasi-bidirectional I/O port (P0–P7), including latched outputs with high-current drive capability for directly driving LEDs. Each quasi-bidirectional I/O can be used as an input or output without the use of a data-direction control signal. At power on, the I/Os are high. In this mode, only a current source to V<sub>CC</sub> is active. An additional strong pullup to V<sub>CC</sub> allows fast rising edges into heavily loaded outputs. This device turns on when an output is written high and is switched off by the negative edge of SCL. The I/Os should be high before being used as inputs.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The PCF8574 provides an open-drain output ( $\overline{\text{INT}}$ ) that can be connected to the interrupt input of a microcontroller. An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time,  $t_{\text{IV}}$ ,  $\overline{\text{INT}}$  is valid. Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from, or written to, the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge bit after the rising edge of the SCL signal, or in the write mode at the acknowledge clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and, after the next rising clock edge, is transmitted as  $\overline{\text{INT}}$ . Reading from, or writing to, another device does not affect the interrupt circuit.

By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I<sup>2</sup>C bus. Therefore, the PCF8574 can remain a simple slave device.

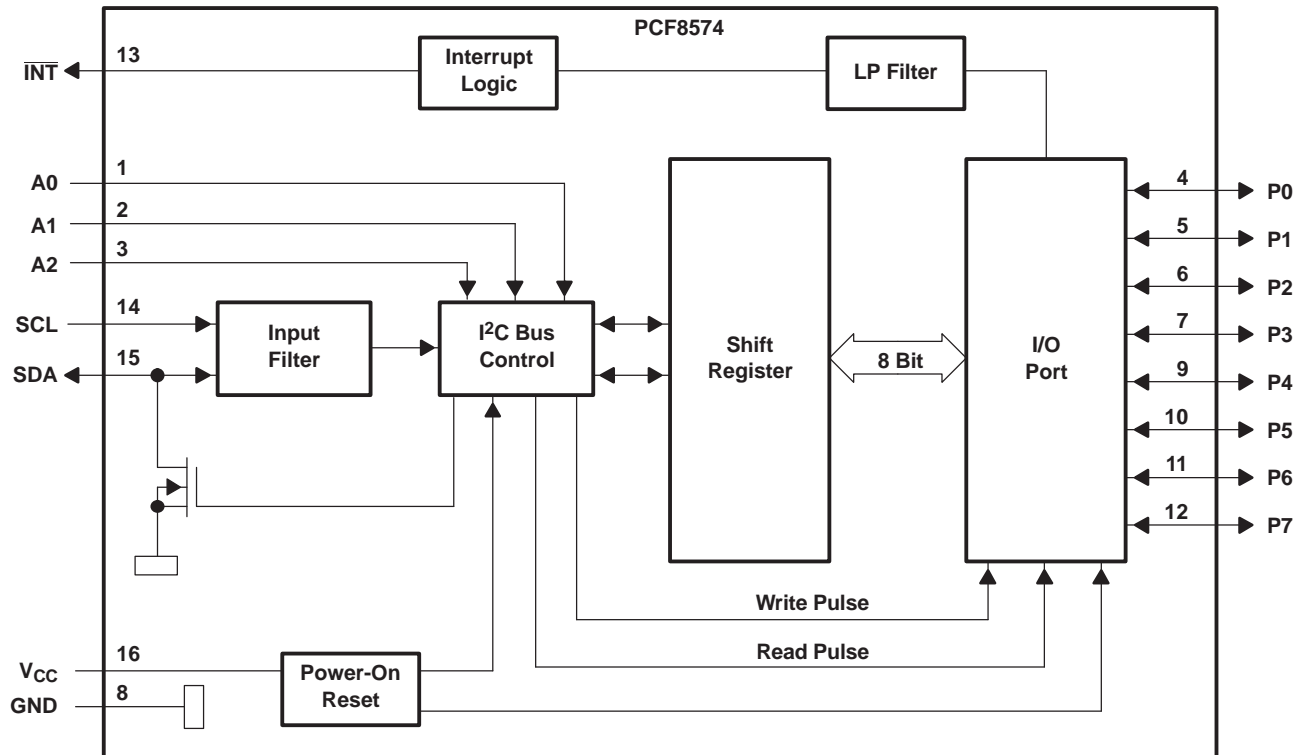
### ORDERING INFORMATION

| $T_A$         | PACKAGE <sup>(1)(2)</sup> |              | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|---------------------------|--------------|-----------------------|------------------|
| –40°C to 85°C | PDIP – N                  | Tube of 25   | PCF8574N              | PCF8574N         |
|               |                           |              | PCF8574NE4            |                  |
|               | QFN – RGT                 | Reel of 3000 | PCF8574RGTR           | ZWJ              |
|               | QFN – RGY                 | Reel of 1000 | PCF8574RGYR           | PF574            |
|               |                           |              | PCF8574RGYRG4         |                  |
|               | SOIC – DW                 | Tube of 40   | PCF8574DW             | PCF8574          |
|               |                           |              | PCF8574DWE4           |                  |
|               |                           | Reel of 2000 | PCF8574DWR            |                  |
|               |                           |              | PCF8574DWRE4          |                  |
|               | TSSOP – PW                | Tube of 70   | PCF8574PW             | PF574            |
|               |                           |              | PCF8574PWE4           |                  |
|               |                           | Reel of 2000 | PCF8574PWR            |                  |
|               |                           |              | PCF8574PWRE4          |                  |
|               | TVSOP – DGV               | Reel of 2000 | PCF8574DGVR           | PF574            |
|               |                           |              | PCF8574DGVRE4         |                  |

(1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

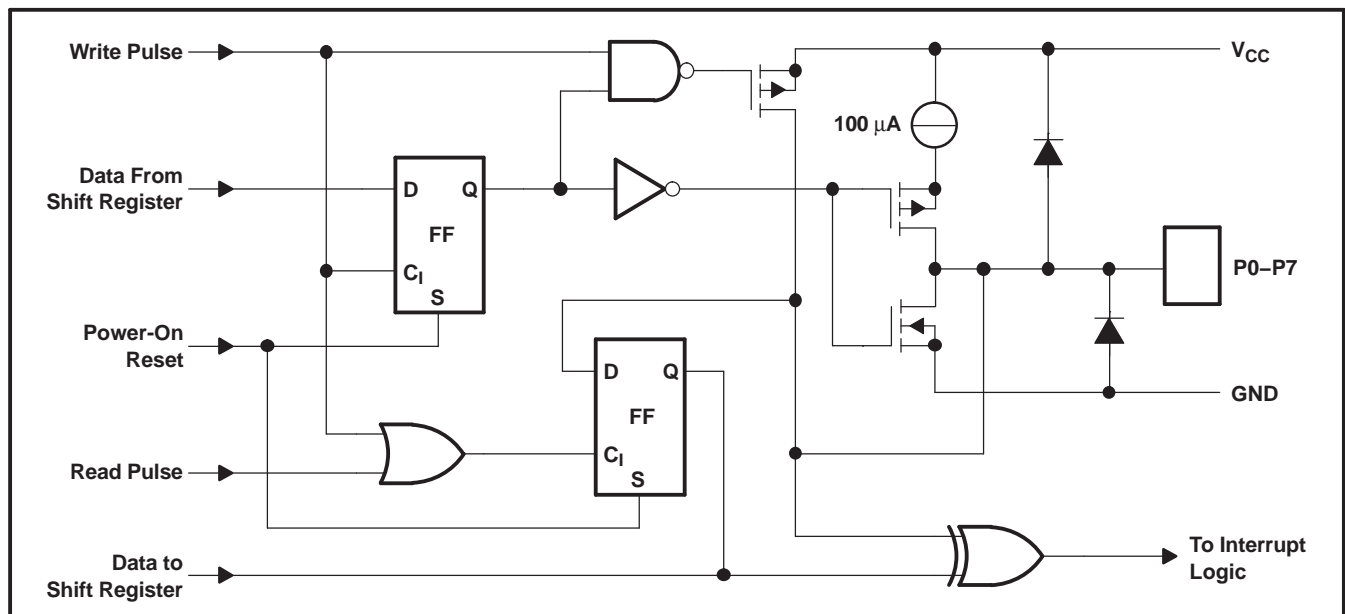
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

## LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DW and N packages.

## SIMPLIFIED SCHEMATIC DIAGRAM OF EACH P-PORT INPUT/OUTPUT



## I<sup>2</sup>C Interface

I<sup>2</sup>C communication with this device is initiated by a master sending a start condition, a high-to-low transition on the SDA I/O while the SCL input is high. After the start condition, the device address byte is sent, most-significant bit (MSB) first, including the data direction bit ( $\overline{R/\overline{W}}$ ). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an acknowledge, a low on the SDA I/O during the high of the acknowledge-related clock pulse. The address inputs (A0–A2) of the slave device must not be changed between the start and the stop conditions.

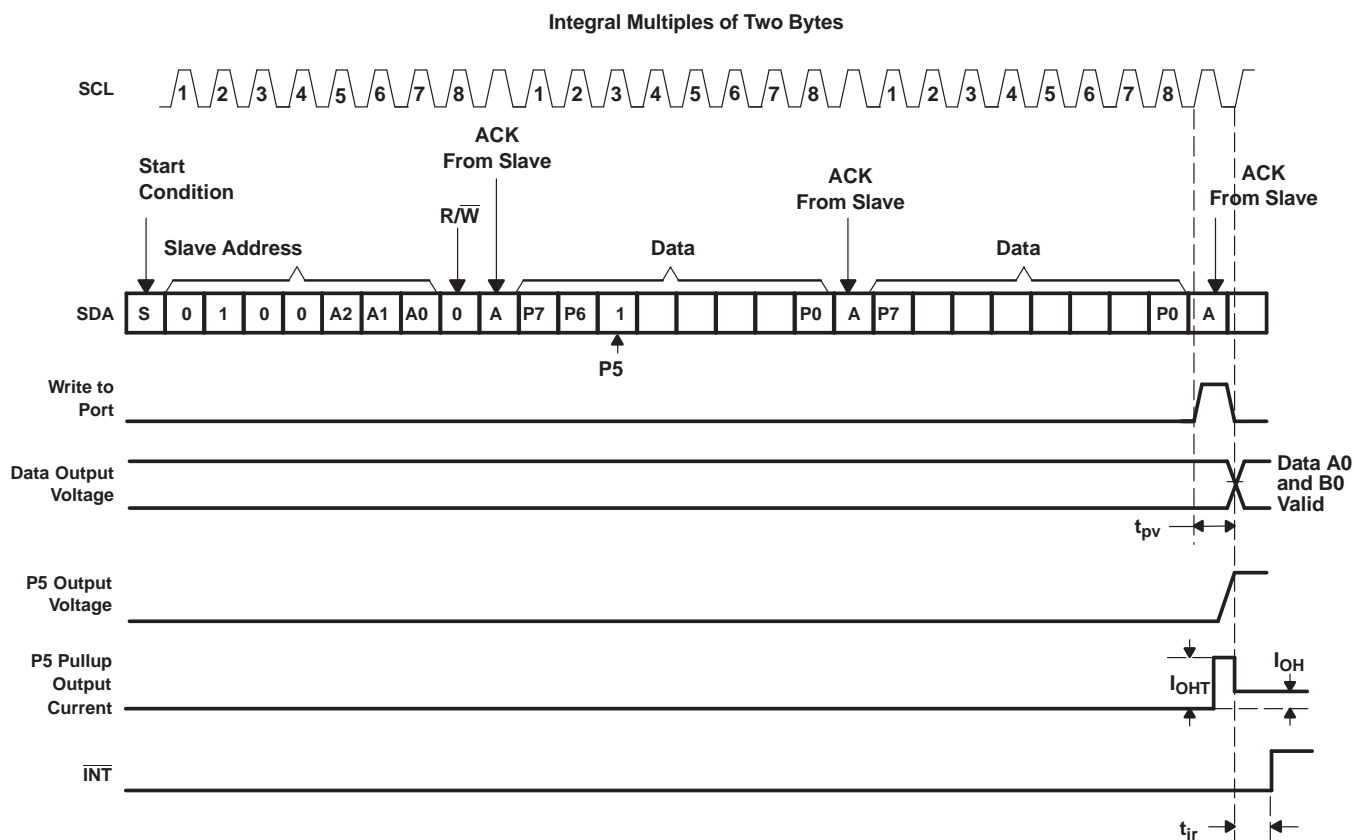
The data byte follows the address acknowledge. If the  $\overline{R/\overline{W}}$  bit is high, the data from this device are the values read from the P port. If the  $\overline{R/\overline{W}}$  bit is low, the data are from the master, to be output to the P port. The data byte is followed by an acknowledge sent from this device. If other data bytes are sent from the master, following the acknowledge, they are ignored by this device. Data are output only if complete bytes are received and acknowledged. The output data will be valid at time,  $t_{pv}$ , after the low-to-high transition of SCL and during the clock cycle for the acknowledge.

A stop condition, which is a low-to-high transition on the SDA I/O while the SCL input is high, is sent by the master.

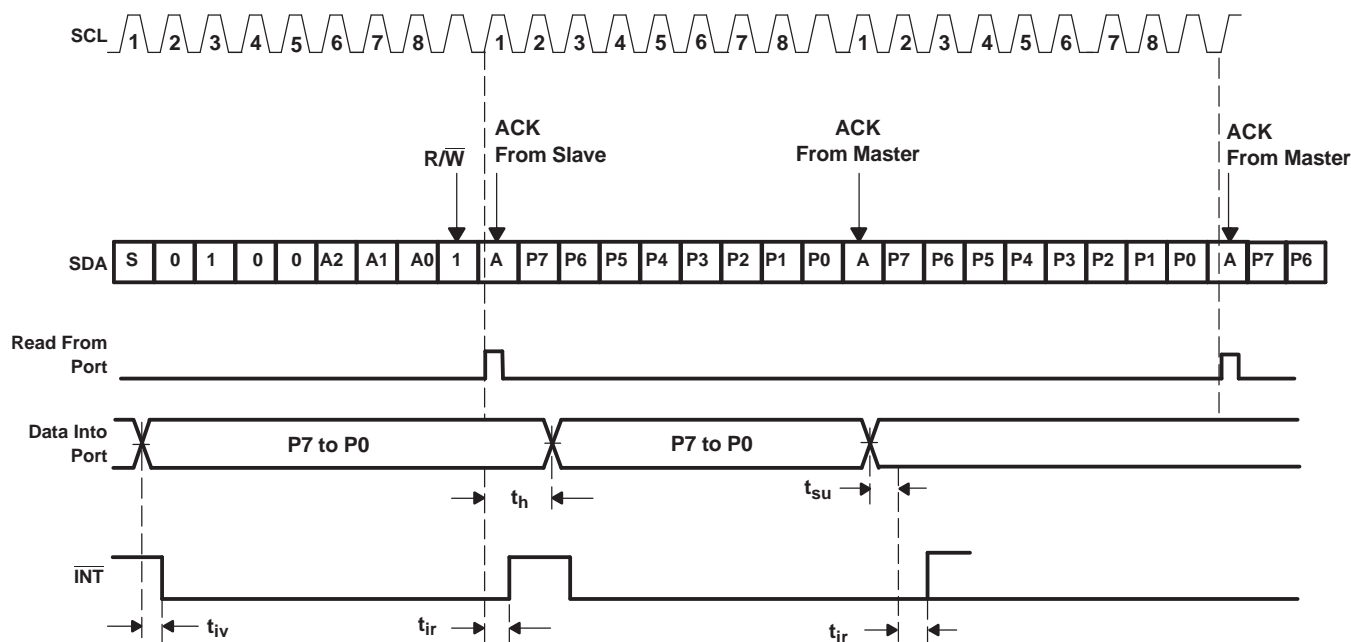
**Interface Definition**

| BYTE                           | BIT     |    |    |    |    |    |    |                             |
|--------------------------------|---------|----|----|----|----|----|----|-----------------------------|
|                                | 7 (MSB) | 6  | 5  | 4  | 3  | 2  | 1  | 0 (LSB)                     |
| I <sup>2</sup> C slave address | L       | H  | L  | L  | A2 | A1 | A0 | $\overline{R/\overline{W}}$ |
| I/O data bus                   | P7      | P6 | P5 | P4 | P3 | P2 | P1 | P0                          |

Figure 1 and Figure 2 show the address and timing diagrams for the write and read modes, respectively.



**Figure 1. Write Mode (Output)**



A low-to-high transition of SDA while SCL is high is defined as the stop condition (P). The transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the latest ACK phase is valid (output mode). Input data is lost.

**Figure 2. Read Mode (Input)**

## Address Reference

| INPUTS |    |    | I <sup>2</sup> C BUS SLAVE ADDRESS |
|--------|----|----|------------------------------------|
| A2     | A1 | A0 |                                    |
| L      | L  | L  | 32 (decimal), 20 (hexadecimal)     |
| L      | L  | H  | 33 (decimal), 21 (hexadecimal)     |
| L      | H  | L  | 34 (decimal), 22 (hexadecimal)     |
| L      | H  | H  | 35 (decimal), 23 (hexadecimal)     |
| H      | L  | L  | 36 (decimal), 24 (hexadecimal)     |
| H      | L  | H  | 37 (decimal), 25 (hexadecimal)     |
| H      | H  | L  | 38 (decimal), 26 (hexadecimal)     |
| H      | H  | H  | 39 (decimal), 27 (hexadecimal)     |

Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|                  |   | MIN  | MAX                   | UNIT    |
|------------------|---|--|-----------------------|---------|
| V <sub>CC</sub>  | Supply voltage range                              | −0.5   | 7                     | V       |
| V <sub>I</sub>   | Input voltage range <sup>(2)</sup>                | −0.5   | V <sub>CC</sub> + 0.5 | V       |
| V <sub>O</sub>   | Output voltage range <sup>(2)</sup>               | −0.5   | V <sub>CC</sub> + 0.5 | V       |
| I <sub>IK</sub>  | Input clamp current                               | V <sub>I</sub> < 0                                     |                       | −20 mA  |
| I <sub>OK</sub>  | Output clamp current                              | V <sub>O</sub> < 0                                     |                       | −20 mA  |
| I <sub>OK</sub>  | Input/output clamp current                        | V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> |                       | ±400 μA |
| I <sub>OL</sub>  | Continuous output low current                     | V <sub>O</sub> = 0 to V <sub>CC</sub>                  |                       | 50 mA   |
| I <sub>OH</sub>  | Continuous output high current                    | V <sub>O</sub> = 0 to V <sub>CC</sub>                  |                       | −4 mA   |
|                  | Continuous current through V <sub>CC</sub> or GND |  |                       | ±100 mA |
| θ <sub>JA</sub>  | Package thermal impedance                         | DGV package <sup>(3)</sup>                             |                       | 92      |
|                  |   | DW package <sup>(3)</sup>                              |                       | 57      |
|                  |   | N package <sup>(3)</sup>                               |                       | 67      |
|                  |   | PW package <sup>(3)</sup>                              |                       | 83      |
|                  |   | RGT package <sup>(4)</sup>                             |                       | 53      |
|                  |   | RGY package <sup>(4)</sup>                             |                       | 37      |
| T <sub>stg</sub> | Storage temperature range                         | −65  | 150                   | °C      |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.
- (4) The package thermal impedance is calculated in accordance with JESD 51-5.

## Recommended Operating Conditions

|                 |                                | MIN                   | MAX                   | UNIT |
|-----------------|--------------------------------|-----------------------|-----------------------|------|
| V <sub>CC</sub> | Supply voltage                 | 2.5                   | 6                     | V    |
| V <sub>IH</sub> | High-level input voltage       | 0.7 × V <sub>CC</sub> | V <sub>CC</sub> + 0.5 | V    |
| V <sub>IL</sub> | Low-level input voltage        | −0.5                  | 0.3 × V <sub>CC</sub> | V    |
| I <sub>OH</sub> | High-level output current      | −1                    |                       | mA   |
| I <sub>OL</sub> | Low-level output current       | 25                    |                       | mA   |
| T <sub>A</sub>  | Operating free-air temperature | −40                   | 85                    | °C   |

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER        |                                       | TEST CONDITIONS   | V <sub>CC</sub> | MIN  | TYP <sup>(1)</sup> | MAX  | UNIT |
|------------------|---------------------------------------|---|-----------------|------|--------------------|------|------|
| V <sub>IK</sub>  | Input diode clamp voltage             | I <sub>I</sub> = –18 mA   | 2.5 V to 6 V    | –1.2 |                    |      | V    |
| V <sub>POR</sub> | Power-on reset voltage <sup>(2)</sup> | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0                             | 6 V             |      | 1.3                | 2.4  | V    |
| I <sub>OH</sub>  | P port                                | V <sub>O</sub> = GND  | 2.5 V to 6 V    | 30   |                    | 300  | μA   |
| I <sub>OHT</sub> | P-port transient pullup current       | High during acknowledge, V <sub>OH</sub> = GND  | 2.5 V           |      | –1                 |      | mA   |
| I <sub>OL</sub>  | SDA                                   | V <sub>O</sub> = 0.4 V  | 2.5 V to 6 V    | 3    |                    |      | mA   |
|                  | P port                                | V <sub>O</sub> = 1 V  | 5 V             | 10   | 25                 |      |      |
|                  | INT                                   | V <sub>O</sub> = 0.4 V  | 2.5 V to 6 V    | 1.6  |                    |      |      |
| I <sub>I</sub>   | SCL, SDA                              | V <sub>I</sub> = V <sub>CC</sub> or GND   | 2.5 V to 6 V    |      |                    | ±5   | μA   |
|                  | INT                                   |   |                 |      |                    | ±5   |      |
|                  | A0, A1, A2                            |   |                 |      |                    | ±5   |      |
| I <sub>IHL</sub> | P port                                | V <sub>I</sub> ≥ V <sub>CC</sub> or V <sub>I</sub> ≤ GND                                | 2.5 V to 6 V    |      |                    | ±400 | μA   |
| I <sub>CC</sub>  | Operating mode                        | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0, f <sub>SCL</sub> = 100 kHz | 6 V             |      | 40                 | 100  | μA   |
|                  | Standby mode                          | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0                             |                 |      | 2.5                | 10   |      |
| C <sub>i</sub>   | SCL                                   | V <sub>I</sub> = V <sub>CC</sub> or GND   | 2.5 V to 6 V    |      | 1.5                | 7    | pF   |
| C <sub>io</sub>  | SDA                                   | V <sub>IO</sub> = V <sub>CC</sub> or GND  | 2.5 V to 6 V    |      | 3                  | 7    | pF   |
|                  | P port                                |   |                 |      | 4                  | 10   |      |

(1) All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

(2) The power-on reset circuit resets the I<sup>2</sup>C-bus logic with V<sub>CC</sub> < V<sub>POR</sub> and sets all I/Os to logic high (with current source to V<sub>CC</sub>).

## I<sup>2</sup>C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

|                  |  |                             | MIN | MAX | UNIT |
|------------------|--|-----------------------------|-----|-----|------|
| f <sub>scl</sub> | I <sup>2</sup> C clock frequency                         |                             | 100 |     | kHz  |
| t <sub>sch</sub> | I <sup>2</sup> C clock high time                         |                             | 4   |     | μs   |
| t <sub>scl</sub> | I <sup>2</sup> C clock low time                          |                             | 4.7 |     | μs   |
| t <sub>sp</sub>  | I <sup>2</sup> C spike time                              |                             | 100 |     | ns   |
| t <sub>sds</sub> | I <sup>2</sup> C serial data setup time                  |                             | 250 |     | ns   |
| t <sub>sdh</sub> | I <sup>2</sup> C serial data hold time                   |                             | 0   |     | ns   |
| t <sub>icr</sub> | I <sup>2</sup> C input rise time                         |                             | 1   |     | μs   |
| t <sub>icf</sub> | I <sup>2</sup> C input fall time                         |                             | 0.3 |     | μs   |
| t <sub>ocf</sub> | I <sup>2</sup> C output fall time (10-pF to 400-pF bus)  |                             | 300 |     | ns   |
| t <sub>buf</sub> | I <sup>2</sup> C bus free time between stop and start    |                             | 4.7 |     | μs   |
| t <sub>sts</sub> | I <sup>2</sup> C start or repeated start condition setup |                             | 4.7 |     | μs   |
| t <sub>sth</sub> | I <sup>2</sup> C start or repeated start condition hold  |                             | 4   |     | μs   |
| t <sub>sps</sub> | I <sup>2</sup> C stop condition setup                    |                             | 4   |     | μs   |
| t <sub>vd</sub>  | Valid data time  | SCL low to SDA output valid | 3.4 |     | μs   |
| C <sub>b</sub>   | I <sup>2</sup> C bus capacitive load                     |                             | 400 |     | pF   |

## Switching Characteristics

over recommended operating free-air temperature range,  $C_L \leq 100$  pF (unless otherwise noted) (see [Figure 4](#))

| PARAMETER |                            | FROM<br>(INPUT) | TO<br>(OUTPUT)   | MIN | MAX | UNIT    |
|-----------|----------------------------|-----------------|------------------|-----|-----|---------|
| $t_{pv}$  | Output data valid          | SCL             | P port           |     | 4   | $\mu s$ |
| $t_{su}$  | Input data setup time      | P port          | SCL              | 0   |     | $\mu s$ |
| $t_h$     | Input data hold time       | P port          | SCL              | 4   |     | $\mu s$ |
| $t_{iv}$  | Interrupt valid time       | P port          | $\overline{INT}$ |     | 4   | $\mu s$ |
| $t_{ir}$  | Interrupt reset delay time | SCL             | $\overline{INT}$ |     | 4   | $\mu s$ |



## PARAMETER MEASUREMENT INFORMATION

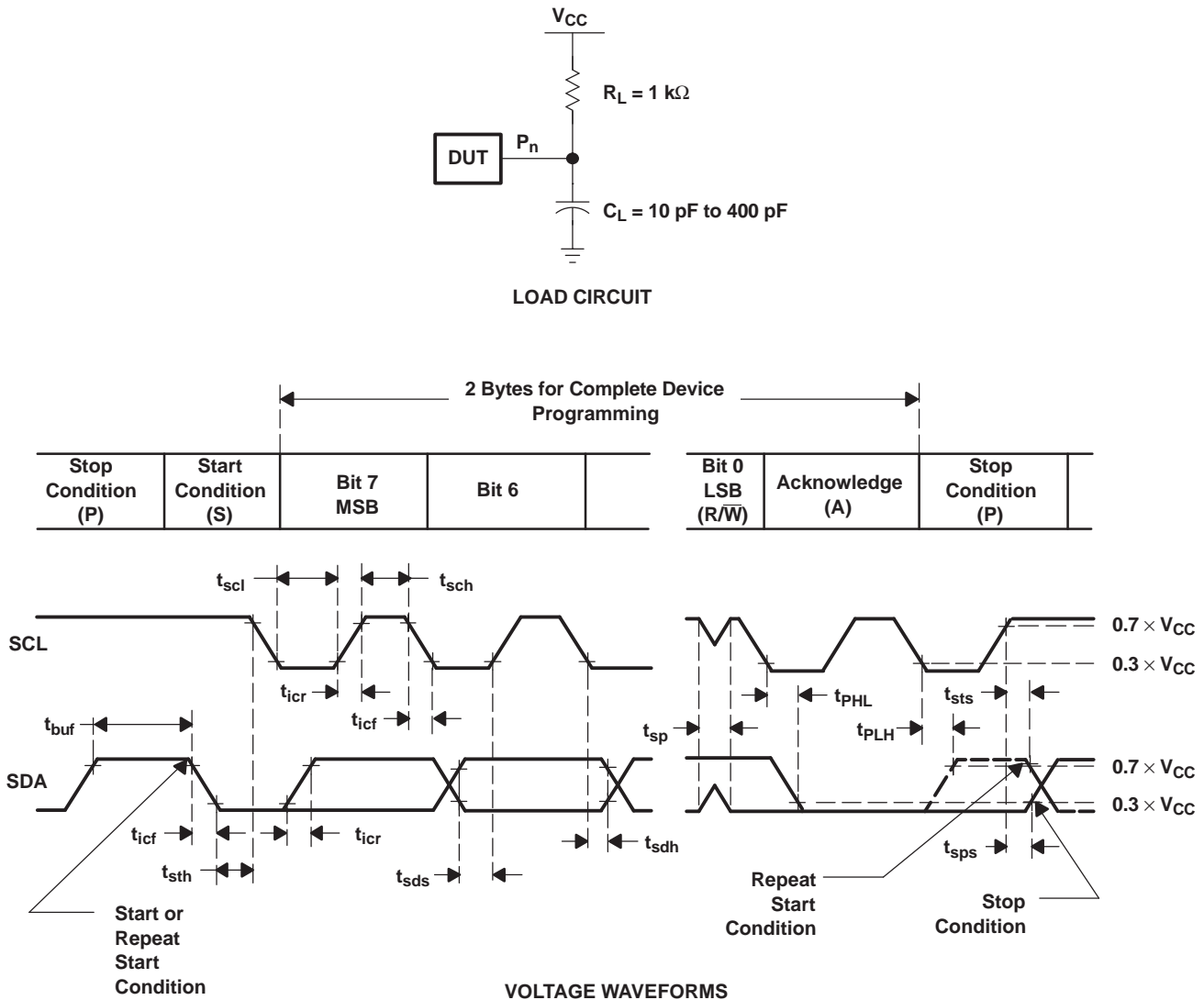
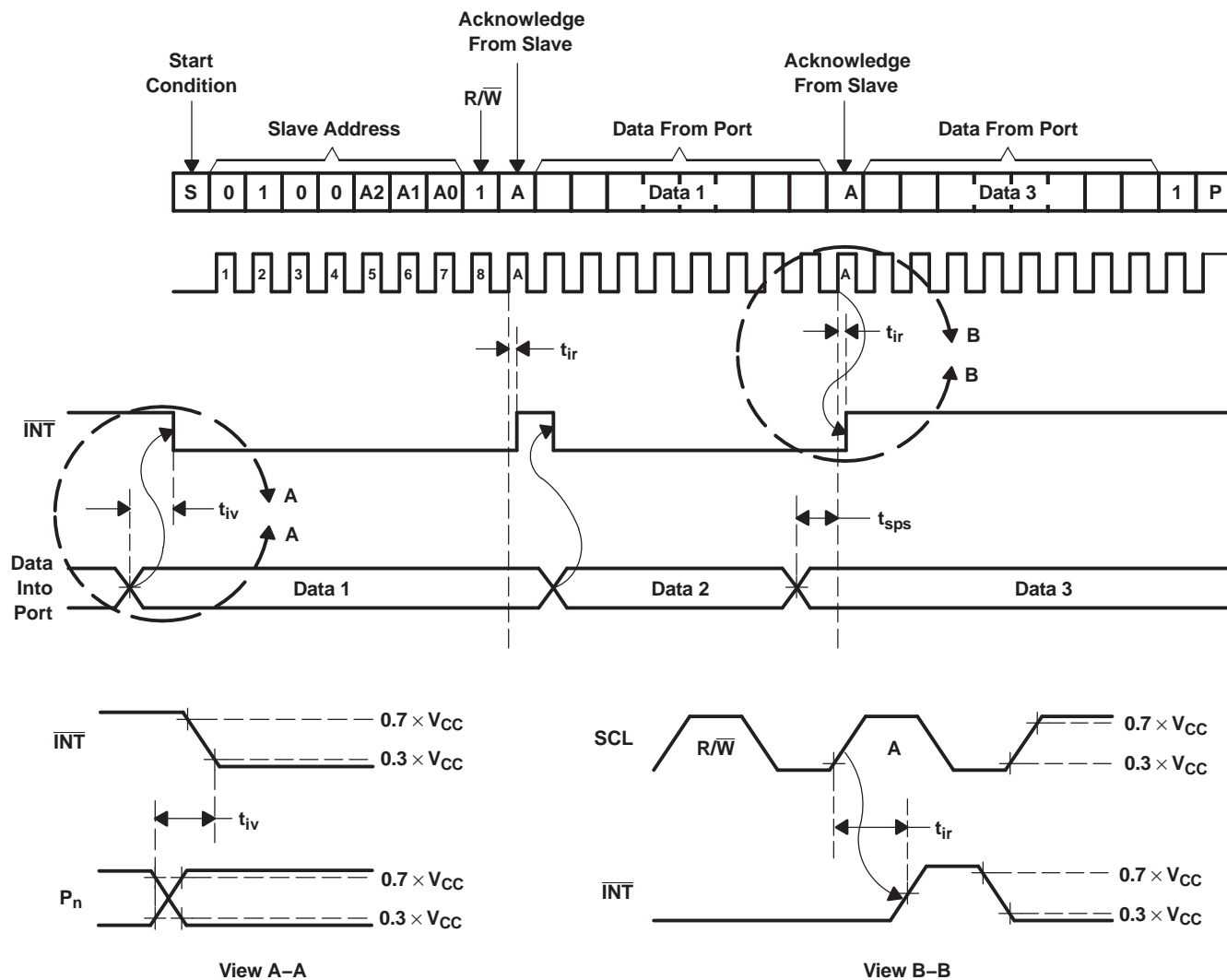
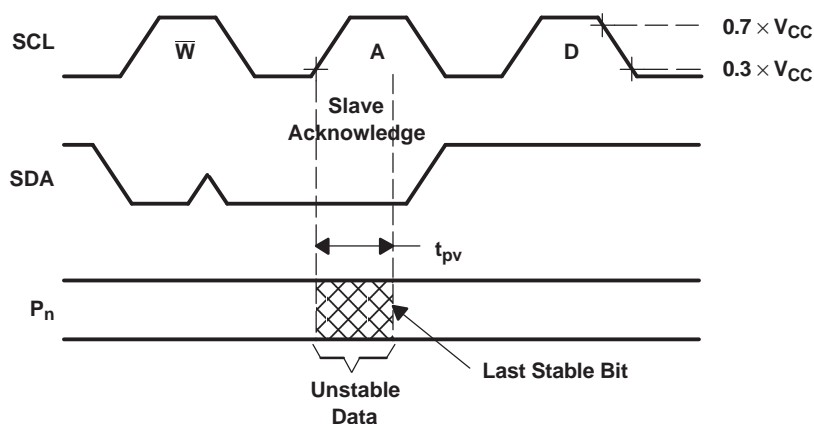
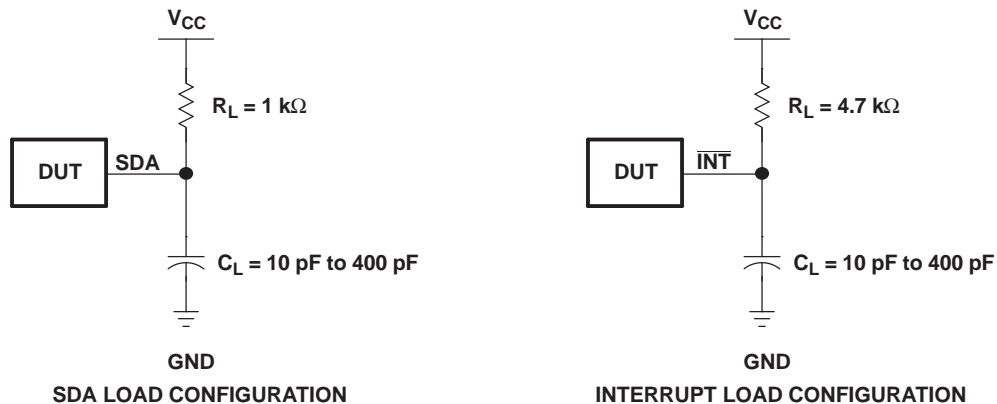


Figure 3. I<sup>2</sup>C Interface Load Circuit and Voltage Waveforms

**PARAMETER MEASUREMENT INFORMATION (continued)****Figure 4. Interrupt Voltage Waveforms****Figure 5. I<sup>2</sup>C Write Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION (continued)



**Figure 6. Load Circuits**

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Top-Side Markings<br>(4) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| PCF8574DGVR      | ACTIVE        | TVSOP        | DGV                | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | PF574                    | <a href="#">Samples</a> |
| PCF8574DGVRE4    | ACTIVE        | TVSOP        | DGV                | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | PF574                    | <a href="#">Samples</a> |
| PCF8574DGVRG4    | ACTIVE        | TVSOP        | DGV                | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | PF574                    | <a href="#">Samples</a> |
| PCF8574DW        | ACTIVE        | SOIC         | DW                 | 16   | 40             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | PCF8574                  | <a href="#">Samples</a> |
| PCF8574DWE4      | ACTIVE        | SOIC         | DW                 | 16   | 40             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | PCF8574                  | <a href="#">Samples</a> |
| PCF8574DWG4      | ACTIVE        | SOIC         | DW                 | 16   | 40             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | PCF8574                  | <a href="#">Samples</a> |
| PCF8574DWR       | ACTIVE        | SOIC         | DW                 | 16   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | PCF8574                  | <a href="#">Samples</a> |
| PCF8574DWRE4     | ACTIVE        | SOIC         | DW                 | 16   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | PCF8574                  | <a href="#">Samples</a> |
| PCF8574DWRG4     | ACTIVE        | SOIC         | DW                 | 16   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | PCF8574                  | <a href="#">Samples</a> |
| PCF8574N         | ACTIVE        | PDIP         | N                  | 16   | 25             | Pb-Free<br>(RoHS)          | CU NIPDAU        | N / A for Pkg Type   | -40 to 85    | PCF8574N                 | <a href="#">Samples</a> |
| PCF8574NE4       | ACTIVE        | PDIP         | N                  | 16   | 25             | Pb-Free<br>(RoHS)          | CU NIPDAU        | N / A for Pkg Type   | -40 to 85    | PCF8574N                 | <a href="#">Samples</a> |
| PCF8574PW        | ACTIVE        | TSSOP        | PW                 | 20   | 70             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | PF574                    | <a href="#">Samples</a> |
| PCF8574PWE4      | ACTIVE        | TSSOP        | PW                 | 20   | 70             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | PF574                    | <a href="#">Samples</a> |
| PCF8574PWG4      | ACTIVE        | TSSOP        | PW                 | 20   | 70             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | PF574                    | <a href="#">Samples</a> |
| PCF8574PWR       | ACTIVE        | TSSOP        | PW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | PF574                    | <a href="#">Samples</a> |
| PCF8574PWRE4     | ACTIVE        | TSSOP        | PW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | PF574                    | <a href="#">Samples</a> |
| PCF8574PWRG4     | ACTIVE        | TSSOP        | PW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | PF574                    | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Top-Side Markings<br>(4) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| PCF8574RGTR      | ACTIVE        | QFN          | RGT                | 16   | 3000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | ZWJ                      | <a href="#">Samples</a> |
| PCF8574RGTRG4    | ACTIVE        | QFN          | RGT                | 16   | 3000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | ZWJ                      | <a href="#">Samples</a> |
| PCF8574RGYR      | ACTIVE        | VQFN         | RGY                | 20   | 3000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR  | -40 to 85    | PF574                    | <a href="#">Samples</a> |
| PCF8574RGYRG4    | ACTIVE        | VQFN         | RGY                | 20   | 3000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR  | -40 to 85    | PF574                    | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| PCF8574DGVR  | TVSOP        | DGV             | 20   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| PCF8574DWR   | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| PCF8574DWRG4 | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| PCF8574PWR   | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |
| PCF8574RGTR  | QFN          | RGT             | 16   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.0     | 8.0     | 12.0   | Q2            |
| PCF8574RGYR  | VQFN         | RGY             | 20   | 3000 | 330.0              | 12.4               | 3.8     | 4.8     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



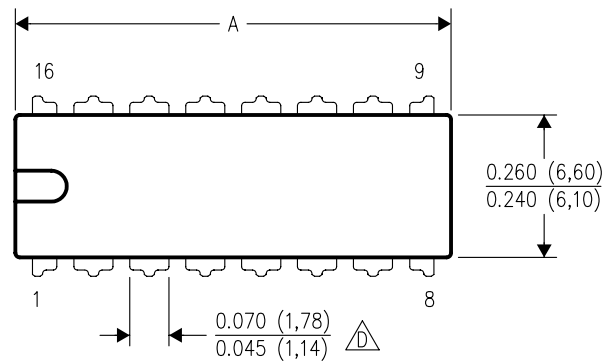
\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| PCF8574DGVR  | TVSOP        | DGV             | 20   | 2000 | 367.0       | 367.0      | 35.0        |
| PCF8574DWR   | SOIC         | DW              | 16   | 2000 | 366.0       | 364.0      | 50.0        |
| PCF8574DWRG4 | SOIC         | DW              | 16   | 2000 | 367.0       | 367.0      | 38.0        |
| PCF8574PWR   | TSSOP        | PW              | 20   | 2000 | 367.0       | 367.0      | 38.0        |
| PCF8574RGTR  | QFN          | RGT             | 16   | 3000 | 346.0       | 346.0      | 35.0        |
| PCF8574RGYR  | VQFN         | RGY             | 20   | 3000 | 367.0       | 367.0      | 35.0        |

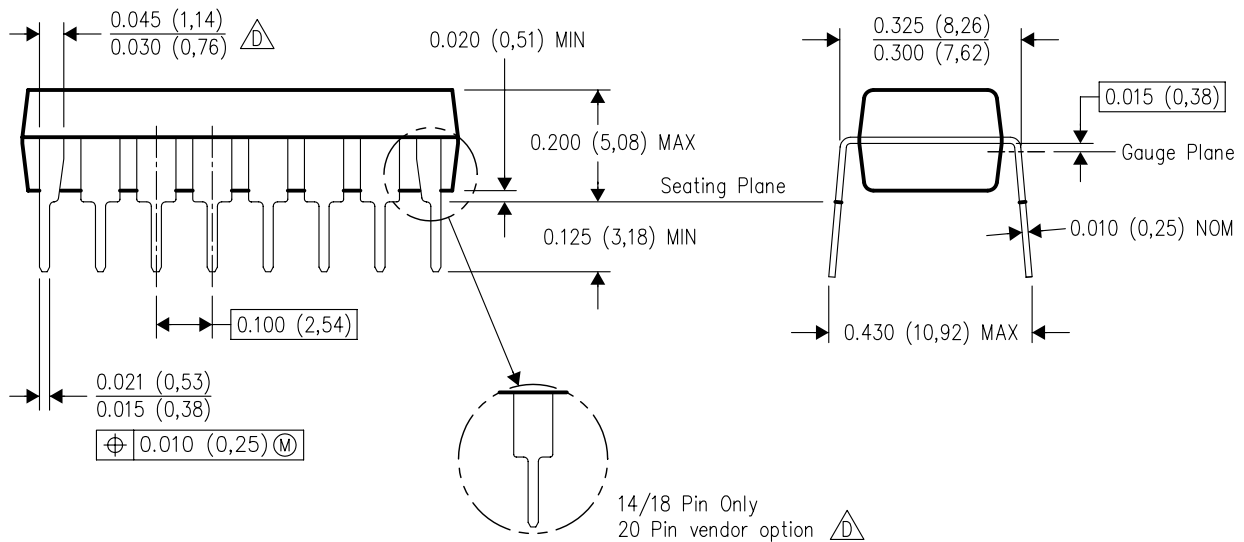
N (R-PDIP-T\*\*)

16 PINS SHOWN

# PLASTIC DUAL-IN-LINE PACKAGE



| DIM \ PINS **       | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



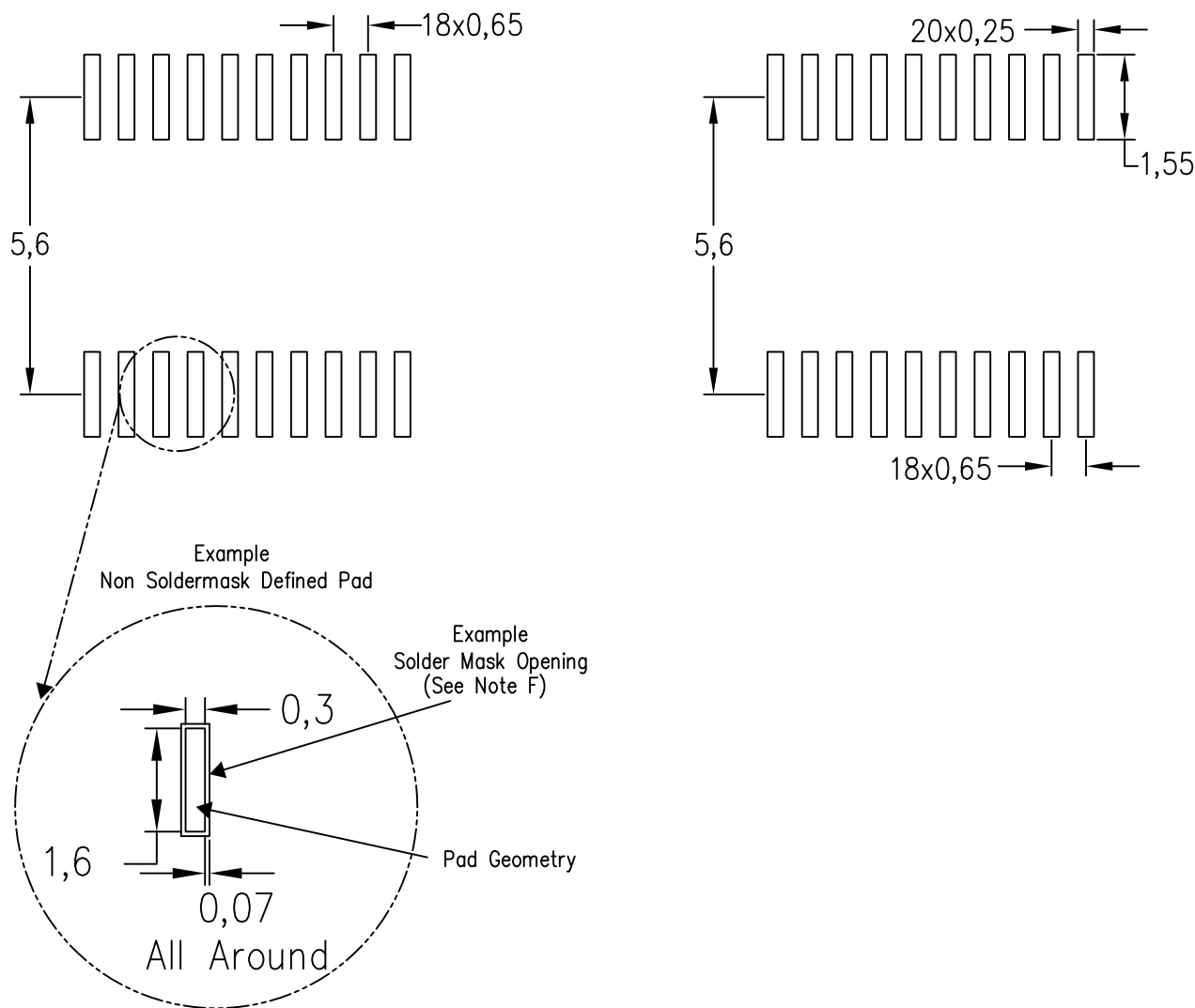
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness  
of .127mm (.005inch).

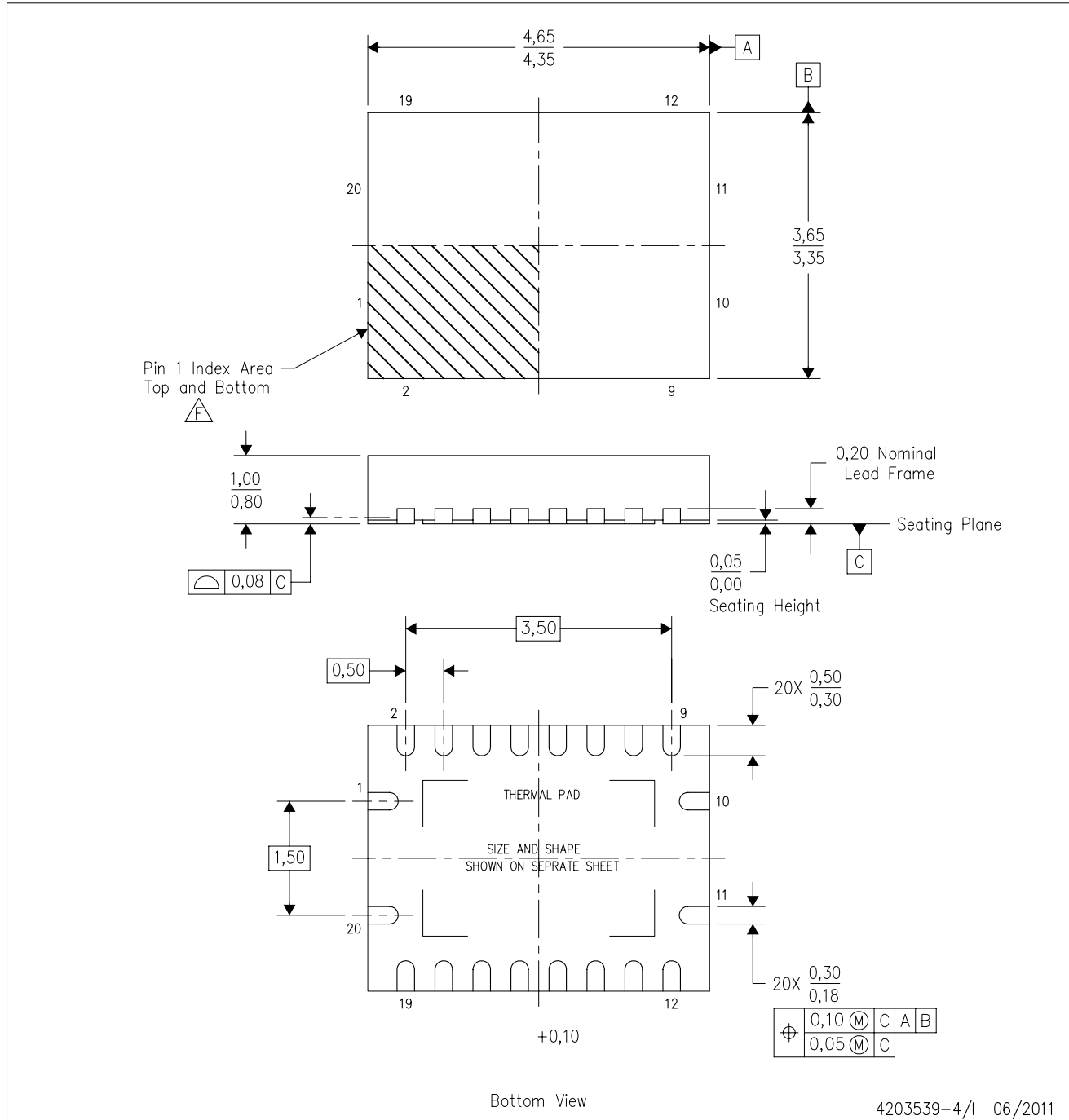


4211284-5/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-4/I 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N20)

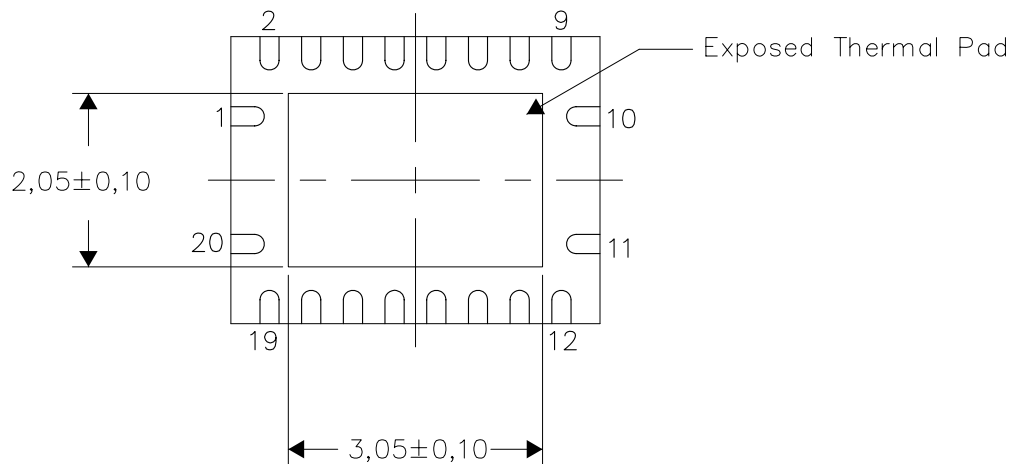
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

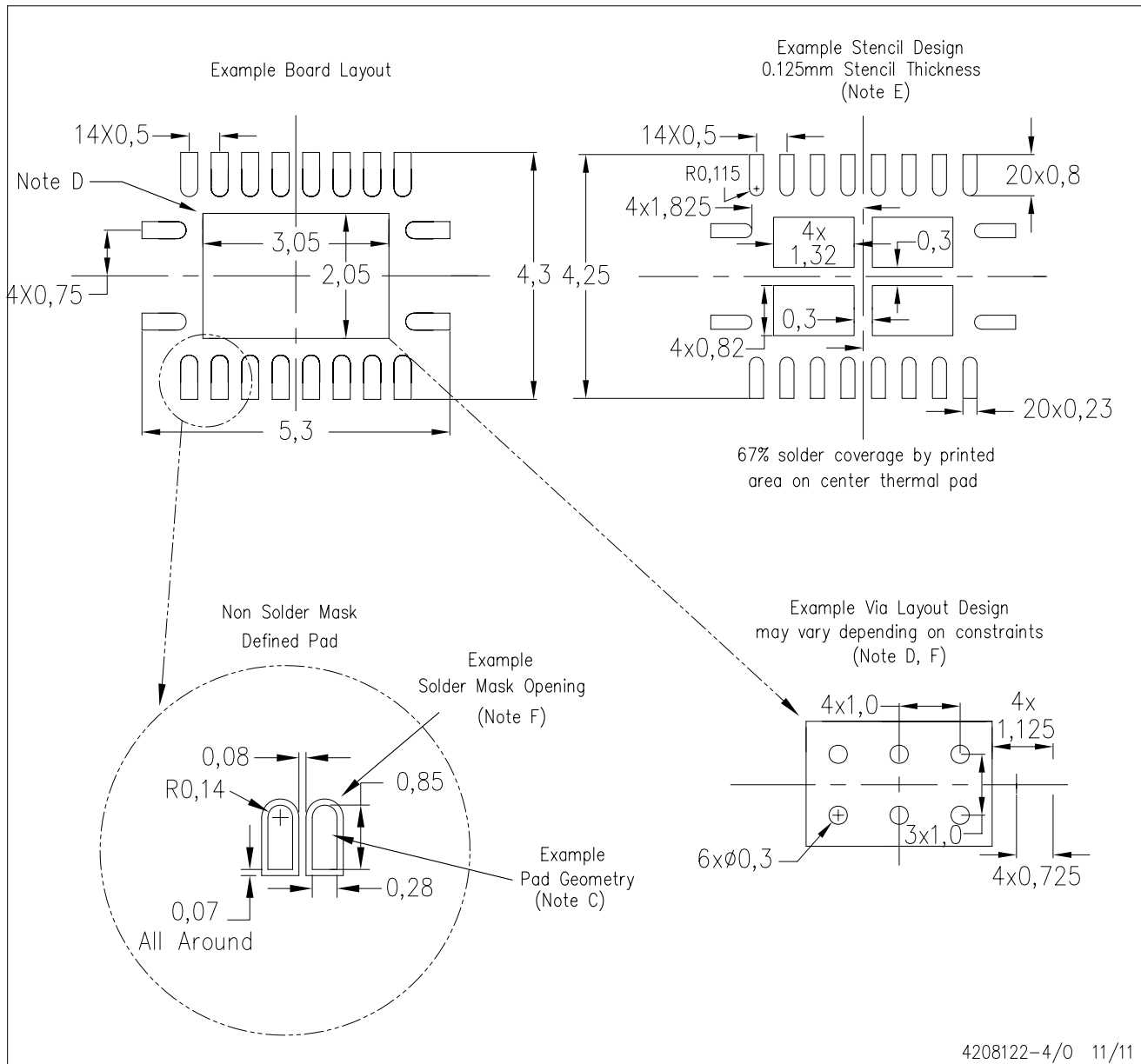
Exposed Thermal Pad Dimensions

4206353-4/0 11/11

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N20)

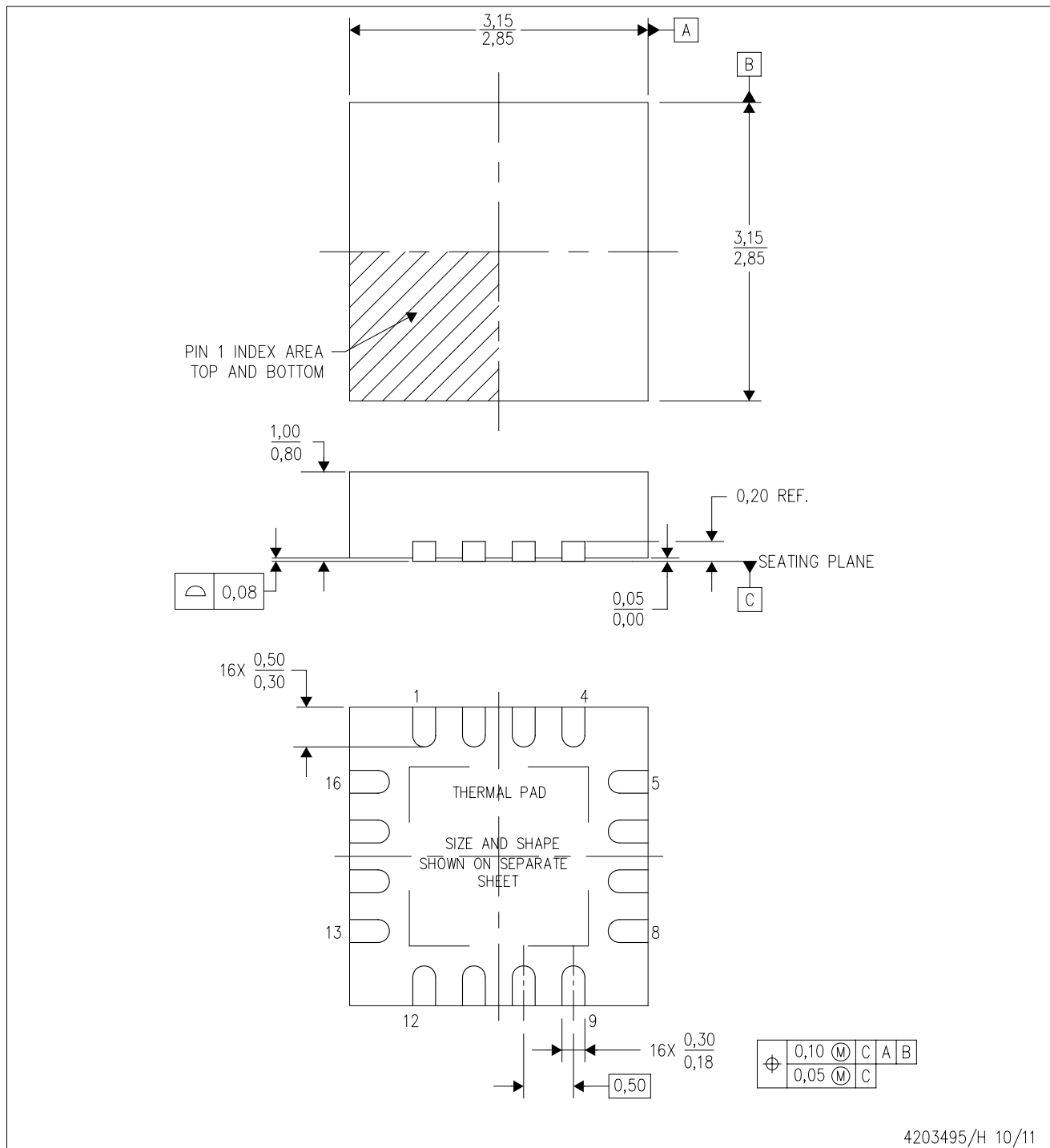
PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203495/H 10/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Quad Flatpack, No-leads (QFN) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-220.

## THERMAL PAD MECHANICAL DATA

RGT (S-PVQFN-N16)

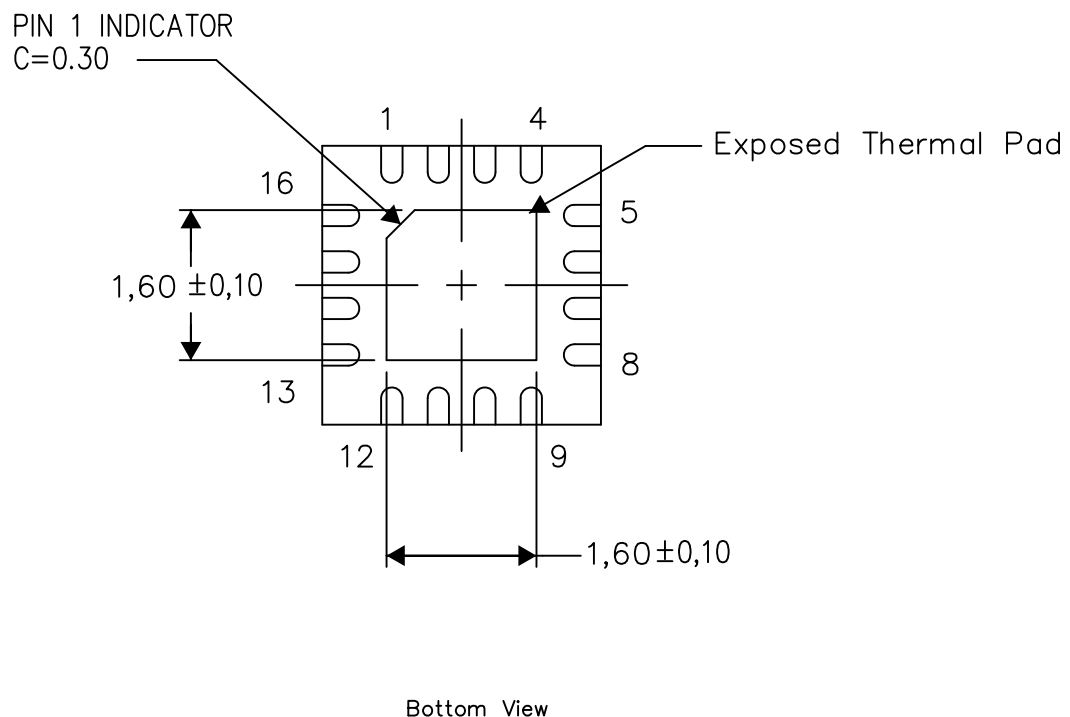
PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

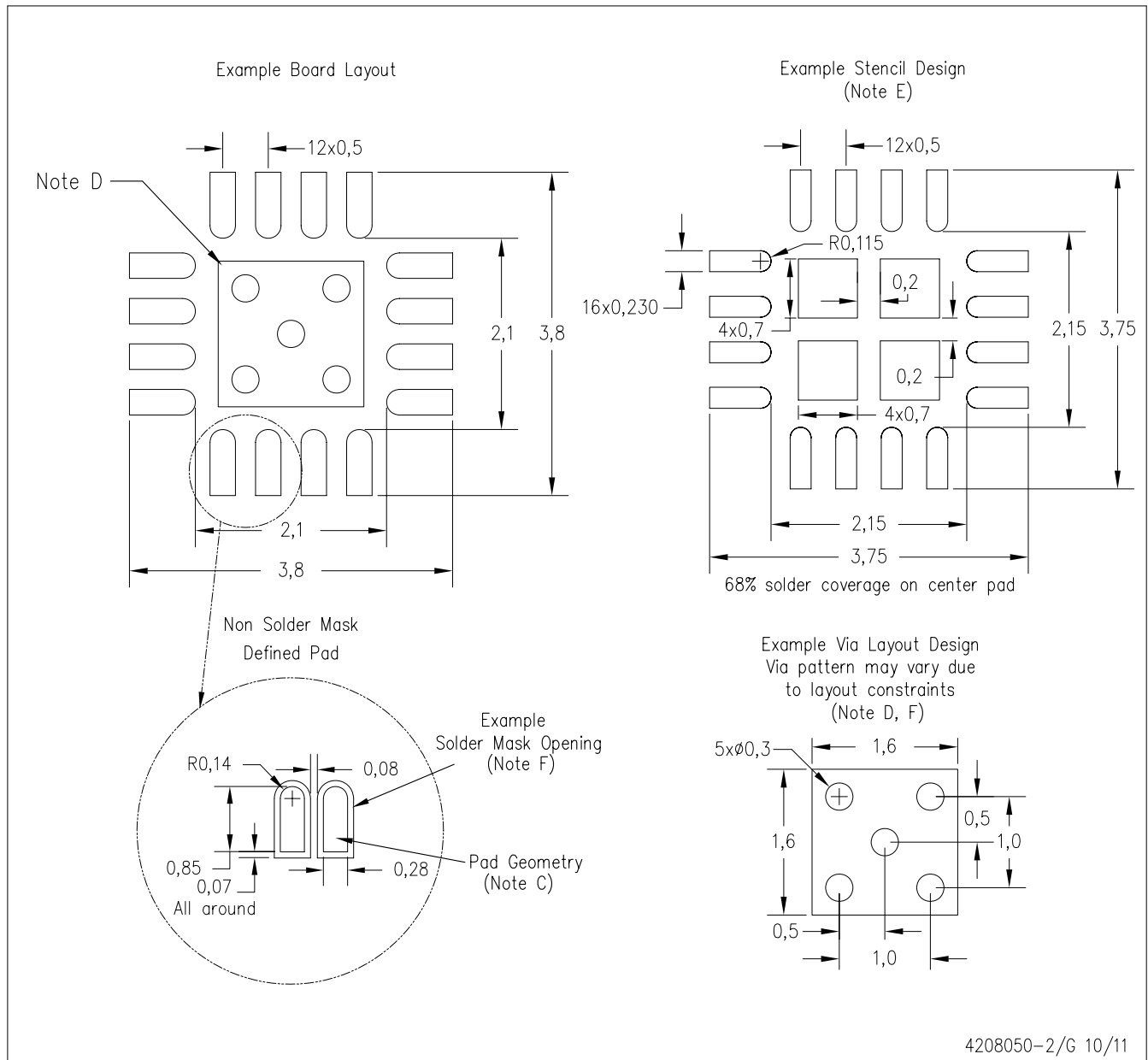
4206349-3/S 04/13

NOTE: All linear dimensions are in millimeters



RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

DW (R-PDSO-G16)

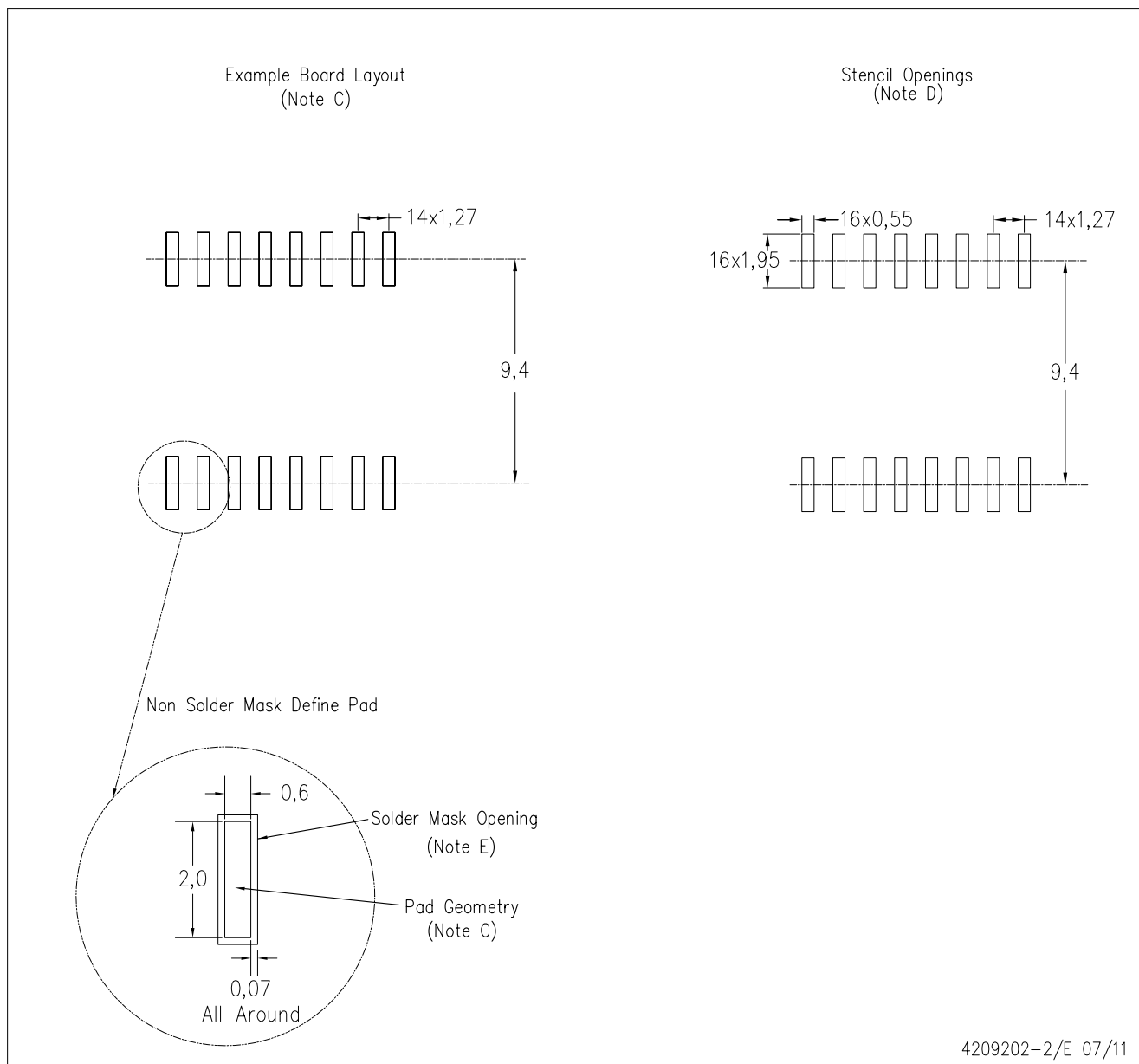
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AA.

DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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