Data Sheet

S6D1121

240 RGB Source & 320 LTPS With GRAM For 262K Colors TFT-LCD

Ver. 1.00

System LSI Division
Semiconductor Business
SAMSUNG ELECTRONICS CO., LTD.

(http://www.samsung.com/Products/Semiconductor/DisplayDriverIC)

CONTENTS

1. DESCRIPTION

S6D1121 is a single chip low power CMOS LCD controller/driver for color LTPS-TFT-LCD displays of 320 gates and 240xRGB columns. It has a 1.38M-bit (240 x 18bit x 320) display RAM and a full set of control functions. S6D1121 offers 10 kinds microprocessor interfaces: 8080-system (8-bit, 9-bit, 16-bit, 18bit), 6800-system (8-bit, 9-bit, 16-bit, 18bit), serial (3-pins) and VSYNC interface. It also supply 18-bit, 16-bit, 6-bit RGB interface for driving Video signal directly from controller.

The S6D1121 supports Qualcomm's high-speed serial interface, MDDI (Mobile Display Digital Interface) type I, which is an implementation of client device Video Electronics Standards Association (VESA) standard.
The MDDI is a cost-effective low-power solution that enables high-speed short-range communication with a display device using a digital packet data link.

The S6D1121 offers interface for sub panel driver IC which doesn't support MDDI: it can generate conventional MPU-interface protocol from MDDI packet.

The S6D1121 has various functions for reducing the power consumption of a LCD system: operating at low voltage (1.5V), register-controlled power-save mode, reduced the power consumption of backlight, partial display mode and so on. The IC has internal GRAM to store 240-RGB x 320 dot 262k-color image and an internal booster that generates the LCD driving voltage, breeder resistance and voltage follower circuit for LCD driver.

This LSI is suitable for any medium-sized or small portable mobile solution requiring long-term driving capabilities, such as digital cellular phones supporting a web browser, bi-directional pagers, and small PDAs.

2. FEATURES

- Single chip LTPS-TFT-LCD Controller/ driver with Display RAM.
- Display resolution: 240*RGB (H) *320(V)
- Display data RAM (frame memory): 240 x 320 x 18-bit = 1,382,400bit
- Output
  - 240ch source outputs
  - Common electrode output
  - LTPS gate control output
- Display mode (Color mode)
  - Full color mode: 262K-colors
  - Reduce color mode: 8-colors (3-bit binary mode)
- Display resolution
  - 240 x 320 Display with 240 x 18-bit x 320 RAM
- MCU Interface
  - VSYNC interface
  - 3-pin serial interface
  - 8-bit, 9-bit, 16-bit, 18-bit interface with 8080-series MCU
  - 8-bit, 9-bit, 16-bit, 18-bit interface with 6800-series MCU
  - 6-bit, 16-bit, 18-bit RGB interface with graphic controller
- MDDI (Mobile Display Digital Interface) support
- Sub Panel Driver IC control function support
  - Conventional LCD driver IC (80/68/STN-mode) can be selected as sub panel driver IC.
- Display features
  - Partial display mode
  - Writing to a window-RAM address area by using a window-address function
  - Software programmable color depth mode
  - Line inversion for low cross talk
- On chip
  - DC/DC converter
  - Adjusted VCOM generation
  - Oscillator for display clock generation
  - Timing generation Non Volatile Memory
- Driving Algorithm
  Line inversion, frame inversion
- Apply voltage range
  - Analog supply voltage range for VCI to VSS: 2.5V to 3.3V
  - I/O supply voltage range for VDD3 to VSS3: 1.65V to 3.3V
- Output voltage levels
  - For the logic part:VDD to VSS = 1.4 to 1.6 V (power supply for logic circuits)
  - For the source driver: AVDD to AVSS = 3.4 to 6.0 V (power supply for driving circuits)
    GVDD to AVSS = 3.0 to 5.0 V (reference power supply for grayscale voltages)
  - For the gate driver: VGH to VGL = 13 to 27 V, VGH to VSSC = +7.5 to +16.0 V,
    VGL to VSSC = -11.0 to -5.5 V.
  - For the step up circuit: VCI1 to VSSC = 1.75 to 3.0 V (refer to Instruction Description)
  - For the LTPS-LCD counter electrode: Vcom amplitude (max) = 5.3V,
    VcomH to AVSS = 3.52 to 5.3V, VcomL to AVSS = 0.0 to 1.0V
- Lower power consumption, suitable for battery operated systems
  - CMOS compatible inputs
  - Optimized layout for COG assembly
  - Operate Temperature range: -40 to +85

3. BLOCK DIAGRAM

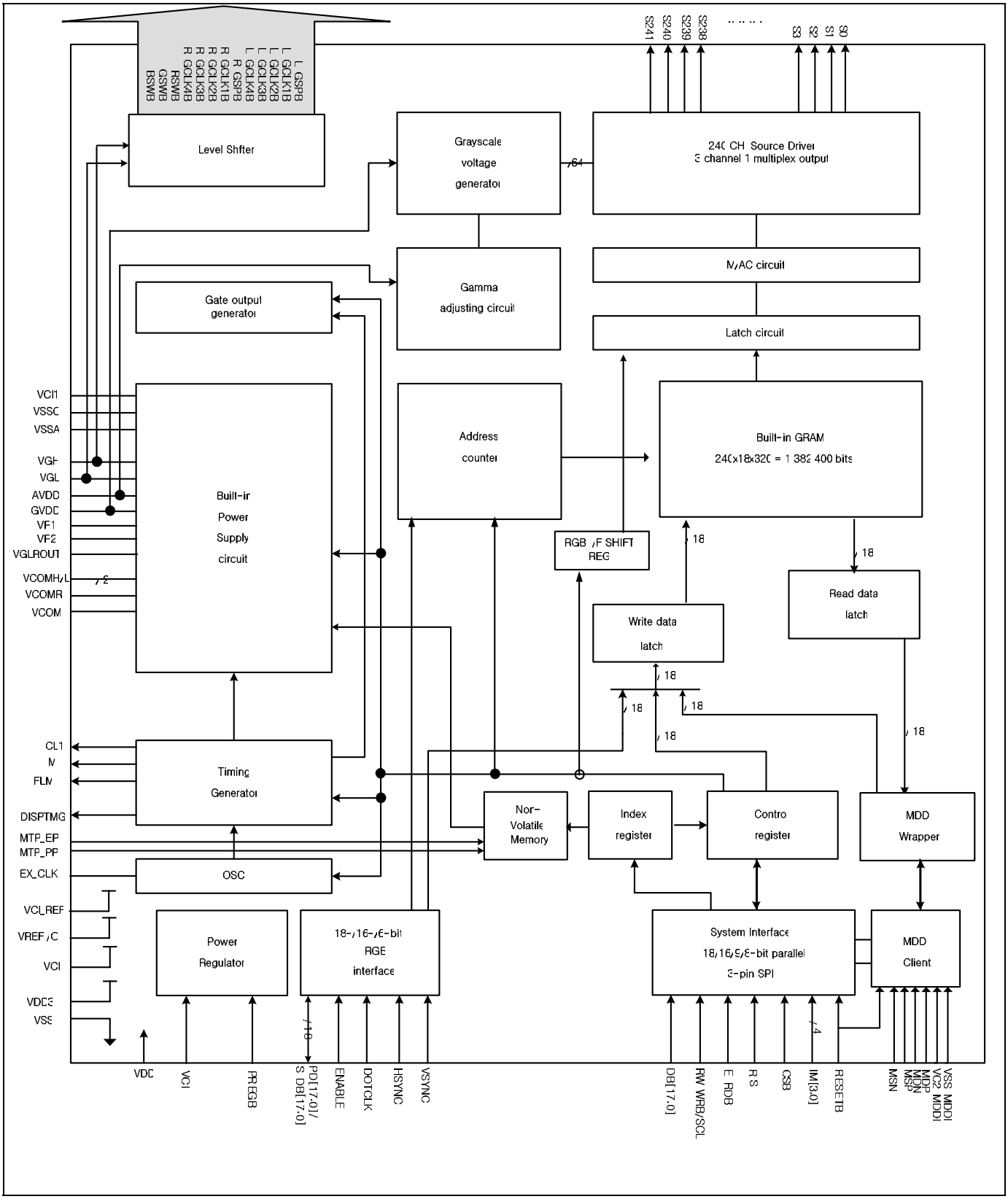


Figure 3.1 S6D1121 Block Diagram

3.1 PAD CONFIGURATION

Table 3.1.1 S6D1121 Pad Dimensions

Items	Pad name.	Size		Unit
		X	Y	
Chip size1)	-	12320	1400	um
Bumped Pad size	Input Pad	30 ±2	100 ± 2	
	Output Pad	25 ± 2	80 ± 2	
Bumped Pad Height	In Wafer	15(typ.) ±3		
	In Chip	Under 2		

NOTES:

1. Scribe line included in this chip size (Scribe lane: 80um)
2. There is a kind of output bumped pads. The dimensions of bumped pads are 25umX80um.

3.2 ALIGN KEY CONFIGURATION AND COORDINATE

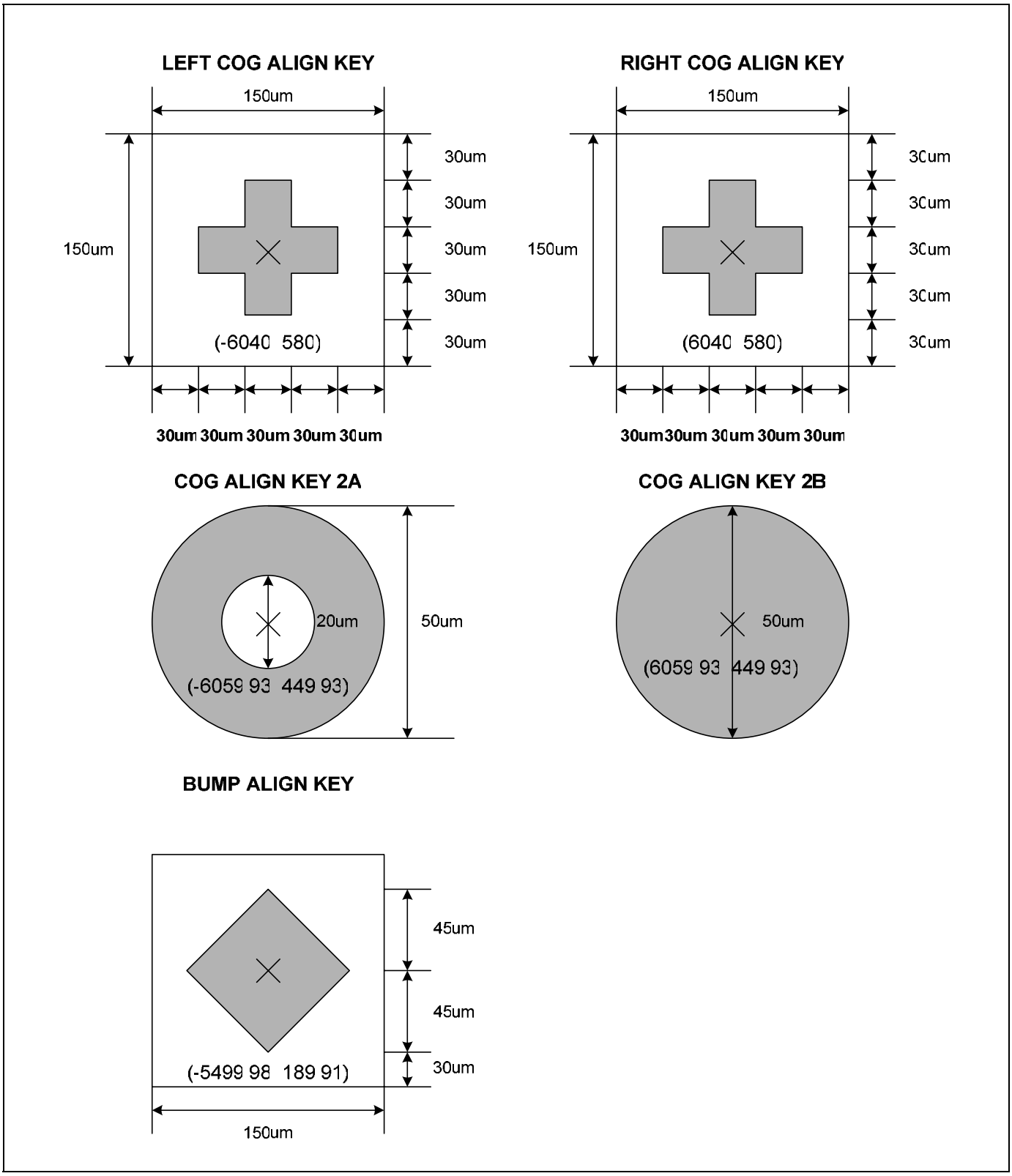


Figure 3.2.1 COG and BUMP align key

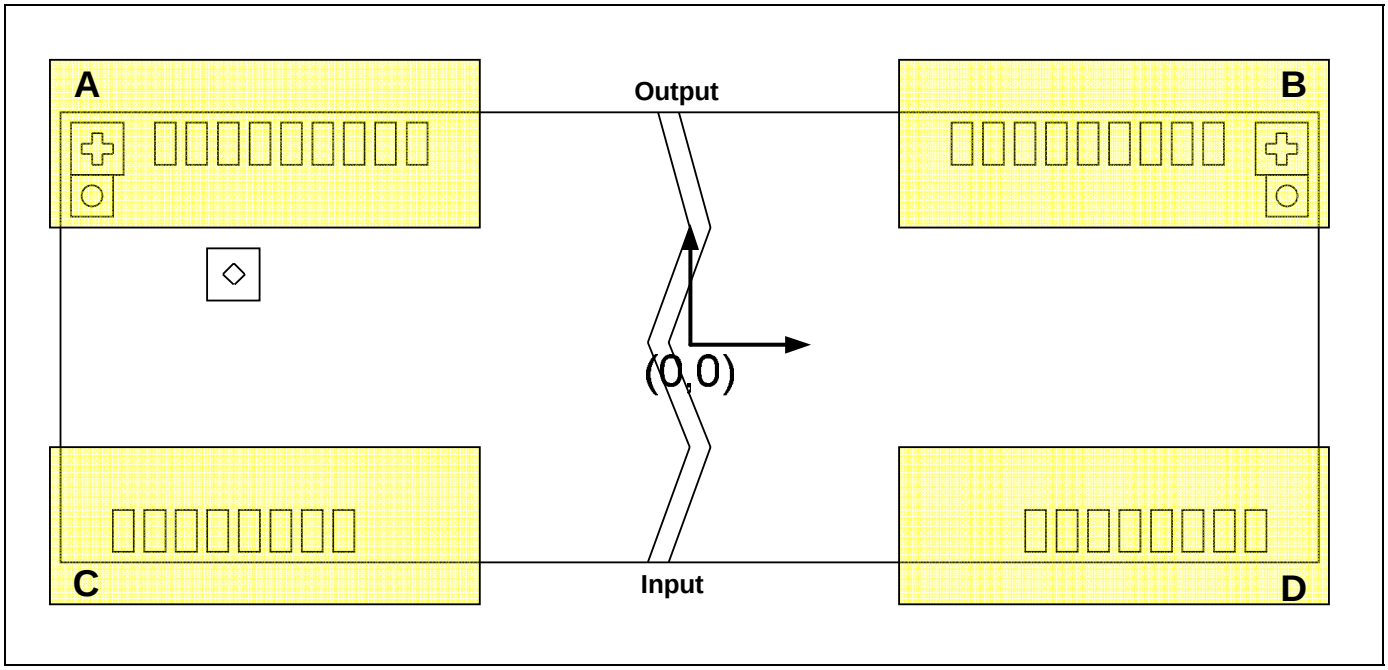


Figure 3.2.2 Align Key Configuration

NOTES:
1. Gold bump height: 15 ± 3 um (typical)
2. Wafer thickness: 300um

3.3 BUMP SIZE

3.3.1 BUMP PAD ARRAY

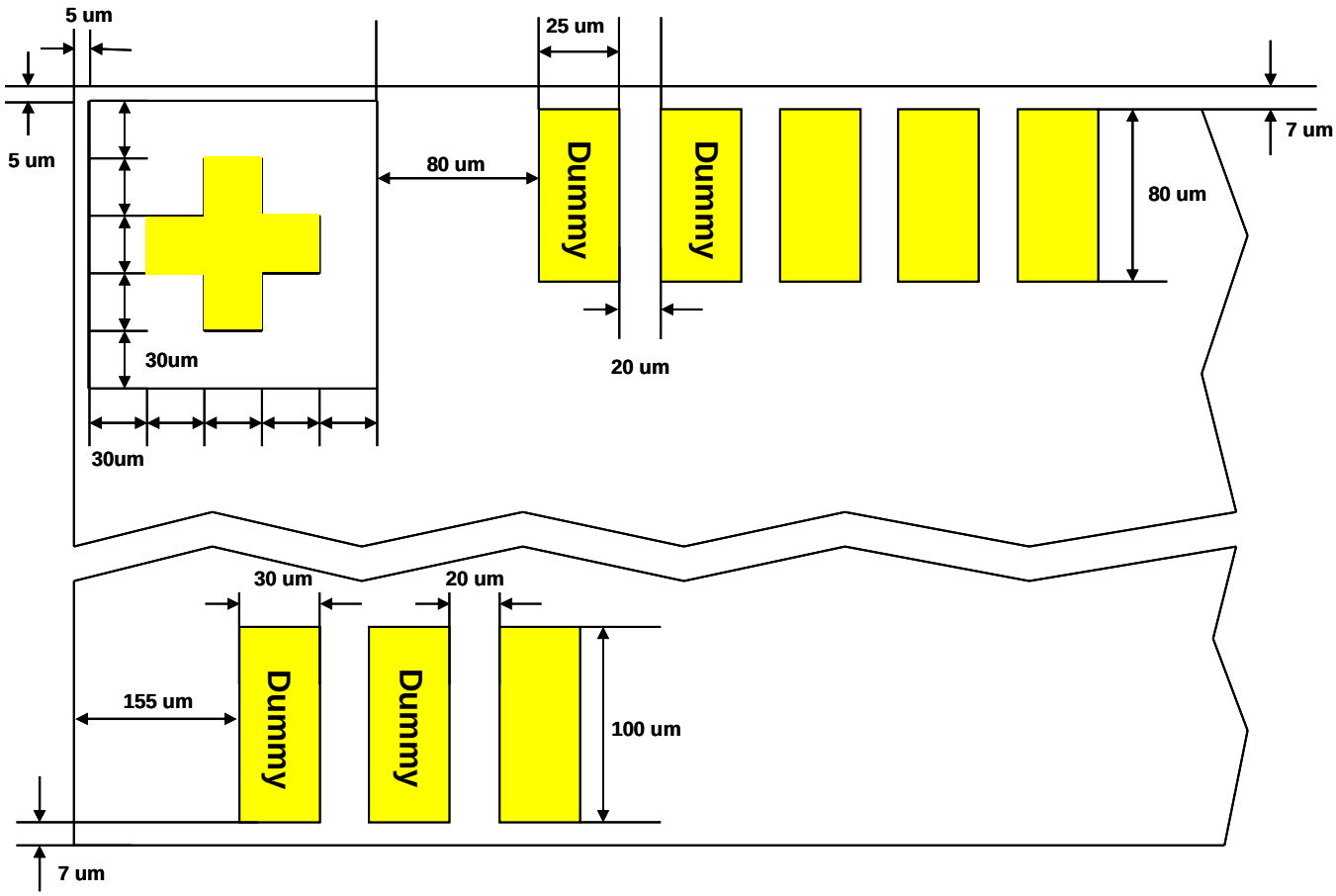


Figure 3.3.1.1 Bump PAD Information

3.4 PAD CENTER COORDINATES

No	PAD Name	X	Y	No	PAD Name	X	Y	No	PAD Name	X	Y
1	DUMMY<1>	-5950	-603	61	C12P	-2950	-603	121	VDD3	50	-603
2	DUMMY<2>	-5900	-603	62	C12M	-2900	-603	122	VSSC	100	-603
3	VCOM	-5850	-603	63	C12M	-2850	-603	123	VSSC	150	-603
4	VCOM	-5800	-603	64	C12M	-2800	-603	124	VSSC	200	-603
5	VCOM	-5750	-603	65	C11P	-2750	-603	125	VSSC	250	-603
6	VCOM	-5700	-603	66	C11P	-2700	-603	126	VSSC	300	-603
7	VCOM	-5650	-603	67	C11P	-2650	-603	127	VSSC	350	-603
8	VCOM	-5600	-603	68	C11P	-2600	-603	128	AVSS	400	-603
9	VCOM	-5550	-603	69	C11P	-2550	-603	129	AVSS	450	-603
10	RESETB	-5500	-603	70	C11M	-2500	-603	130	AVSS	500	-603
11	C21P	-5450	-603	71	C11M	-2450	-603	131	AVSS	550	-603
12	C21P	-5400	-603	72	C11M	-2400	-603	132	AVSS	600	-603
13	C21P	-5350	-603	73	C11M	-2350	-603	133	AVSS	650	-603
14	C21M	-5300	-603	74	C11M	-2300	-603	134	VSS3	700	-603
15	C21M	-5250	-603	75	AVDD	-2250	-603	135	VSS3	750	-603
16	C21M	-5200	-603	76	AVDD	-2200	-603	136	VSS3	800	-603
17	C22P	-5150	-603	77	AVDD	-2150	-603	137	VSS3	850	-603
18	C22P	-5100	-603	78	AVDD	-2100	-603	138	VSS3	900	-603
19	C22P	-5050	-603	79	AVDD	-2050	-603	139	VSS	950	-603
20	C22M	-5000	-603	80	AVDD	-2000	-603	140	VSS	1000	-603
21	C22M	-4950	-603	81	VCI_REF	-1950	-603	141	VSS	1050	-603
22	C22M	-4900	-603	82	VCI	-1900	-603	142	VSS	1100	-603
23	VGH	-4850	-603	83	VCI	-1850	-603	143	VSS	1150	-603
24	VGH	-4800	-603	84	VCI	-1800	-603	144	VSS	1200	-603
25	VGH	-4750	-603	85	VCI	-1750	-603	145	EX_CLK	1250	-603
26	VGH	-4700	-603	86	VCI	-1700	-603	146	TEST_EXCLK_EN	1300	-603
27	VGH	-4650	-603	87	VCI	-1650	-603	147	IM<3>	1350	-603
28	VGH	-4600	-603	88	VCI_MDDI	-1600	-603	148	IM<2>	1400	-603
29	DUMMY<3>	-4550	-603	89	VCI_MDDI	-1550	-603	149	IM<1>	1450	-603
30	VGLROUT	-4500	-603	90	VCI_MDDI	-1500	-603	150	IM<0>	1500	-603
31	VGLROUT	-4450	-603	91	VCI_MDDI	-1450	-603	151	RESETB	1550	-603
32	VGLROUT	-4400	-603	92	MDP	-1400	-603	152	PREGB	1600	-603
33	VGLROUT	-4350	-603	93	MDP	-1350	-603	153	DB<17>	1650	-603
34	VGLROUT	-4300	-603	94	MDN	-1300	-603	154	DB<16>	1700	-603
35	VGLROUT	-4250	-603	95	MDN	-1250	-603	155	DB<15>	1750	-603
36	VGL	-4200	-603	96	MSP	-1200	-603	156	DB<14>	1800	-603
37	VGL	-4150	-603	97	MSP	-1150	-603	157	DB<13>	1850	-603
38	VGL	-4100	-603	98	MSN	-1100	-603	158	DB<12>	1900	-603
39	VGL	-4050	-603	99	MSN	-1050	-603	159	DB<11>	1950	-603
40	VGL	-4000	-603	100	VSS_MDDI	-1000	-603	160	DB<10>	2000	-603
41	VGL	-3950	-603	101	VSS_MDDI	-950	-603	161	DB<9>	2050	-603
42	DUMMY<4>	-3900	-603	102	VSS_MDDI	-900	-603	162	DB<8>	2100	-603
43	DUMMY<5>	-3850	-603	103	VSS_MDDI	-850	-603	163	DB<7>	2150	-603
44	VR1	-3800	-603	104	DUMMY<6>	-800	-603	164	DB<6>	2200	-603
45	VR1	-3750	-603	105	VGS	-750	-603	165	DB<5>	2250	-603
46	VR1	-3700	-603	106	VGS	-700	-603	166	DB<4>	2300	-603
47	VR1	-3650	-603	107	VDD	-650	-603	167	DB<3>	2350	-603
48	VR1	-3600	-603	108	VDD	-600	-603	168	DB<2>	2400	-603
49	VR2	-3550	-603	109	VDD	-550	-603	169	DB<1>	2450	-603
50	VR2	-3500	-603	110	VDD	-500	-603	170	DB<0>	2500	-603
51	VR2	-3450	-603	111	VDD	-450	-603	171	E_RDB	2550	-603
52	VR2	-3400	-603	112	VDD	-400	-603	172	RW_WRB	2600	-603
53	VR2	-3350	-603	113	VDD	-350	-603	173	RS	2650	-603
54	VCI1	-3300	-603	114	VDD	-300	-603	174	CSB	2700	-603
55	VCI1	-3250	-603	115	VDD	-250	-603	175	VSYNC	2750	-603
56	VCI1	-3200	-603	116	VDD	-200	-603	176	HSYNC	2800	-603
57	VCI1	-3150	-603	117	VDD3	-150	-603	177	DOTCLK	2850	-603
58	VCI1	-3100	-603	118	VDD3	-100	-603	178	ENABLE	2900	-603
59	C12P	-3050	-603	119	VDD3	-50	-603	179	PD<17>	2950	-603
60	C12P	-3000	-603	120	VDD3	0	-603	180	PD<16>	3000	-603

No	PAD Name	X	Y	No	PAD Name	X	Y	No	PAD Name	X	Y
181	PD<15>	3050	-603	241	DUMMY<10>	5827.5	613	301	S<190>	3127.5	613
182	PD<14>	3100	-603	242	R_GSPB	5782.5	613	302	S<189>	3082.5	613
183	PD<13>	3150	-603	243	R_GCLK1B	5737.5	613	303	S<188>	3037.5	613
184	PD<12>	3200	-603	244	R_GCLK2B	5692.5	613	304	S<187>	2992.5	613
185	PD<11>	3250	-603	245	R_GCLK3B	5647.5	613	305	S<186>	2947.5	613
186	PD<10>	3300	-603	246	R_GCLK4B	5602.5	613	306	S<185>	2902.5	613
187	PD<9>	3350	-603	247	DUMMY<12>	5557.5	613	307	S<184>	2857.5	613
188	PD<8>	3400	-603	248	DUMMY<13>	5512.5	613	308	S<183>	2812.5	613
189	PD<7>	3450	-603	249	DUMMY<14>	5467.5	613	309	S<182>	2767.5	613
190	PD<6>	3500	-603	250	S<241>	5422.5	613	310	S<181>	2722.5	613
191	PD<5>	3550	-603	251	S<240>	5377.5	613	311	S<180>	2677.5	613
192	PD<4>	3600	-603	252	S<239>	5332.5	613	312	S<179>	2632.5	613
193	PD<3>	3650	-603	253	S<238>	5287.5	613	313	S<178>	2587.5	613
194	PD<2>	3700	-603	254	S<237>	5242.5	613	314	S<177>	2542.5	613
195	PD<1>	3750	-603	255	S<236>	5197.5	613	315	S<176>	2497.5	613
196	PD<0>	3800	-603	256	S<235>	5152.5	613	316	S<175>	2452.5	613
197	TEST_MODE<2>	3850	-603	257	S<234>	5107.5	613	317	S<174>	2407.5	613
198	TEST_MODE<1>	3900	-603	258	S<233>	5062.5	613	318	S<173>	2362.5	613
199	TEST_MODE<0>	3950	-603	259	S<232>	5017.5	613	319	S<172>	2317.5	613
200	DISPTMG	4000	-603	260	S<231>	4972.5	613	320	S<171>	2272.5	613
201	PREC	4050	-603	261	S<230>	4927.5	613	321	S<170>	2227.5	613
202	EQ	4100	-603	262	S<229>	4882.5	613	322	S<169>	2182.5	613
203	M	4150	-603	263	S<228>	4837.5	613	323	S<168>	2137.5	613
204	FLM	4200	-603	264	S<227>	4792.5	613	324	S<167>	2092.5	613
205	CL1	4250	-603	265	S<226>	4747.5	613	325	S<166>	2047.5	613
206	TSO<1>	4300	-603	266	S<225>	4702.5	613	326	S<165>	2002.5	613
207	TSO<0>	4350	-603	267	S<224>	4657.5	613	327	S<164>	1957.5	613
208	DUMMY<7>	4400	-603	268	S<223>	4612.5	613	328	S<163>	1912.5	613
209	MTP_PP	4450	-603	269	S<222>	4567.5	613	329	S<162>	1867.5	613
210	MTP_EP	4500	-603	270	S<221>	4522.5	613	330	S<161>	1822.5	613
211	VCOML	4550	-603	271	S<220>	4477.5	613	331	S<160>	1777.5	613
212	VCOML	4600	-603	272	S<219>	4432.5	613	332	S<159>	1732.5	613
213	VCOML	4650	-603	273	S<218>	4387.5	613	333	S<158>	1687.5	613
214	VCOMH	4700	-603	274	S<217>	4342.5	613	334	S<157>	1642.5	613
215	VCOMH	4750	-603	275	S<216>	4297.5	613	335	S<156>	1597.5	613
216	VCOMH	4800	-603	276	S<215>	4252.5	613	336	S<155>	1552.5	613
217	VCOMR	4850	-603	277	S<214>	4207.5	613	337	S<154>	1507.5	613
218	GVDD	4900	-603	278	S<213>	4162.5	613	338	S<153>	1462.5	613
219	GVDD	4950	-603	279	S<212>	4117.5	613	339	S<152>	1417.5	613
220	VCOM_PREC	5000	-603	280	S<211>	4072.5	613	340	S<151>	1372.5	613
221	VCOM_PREC	5050	-603	281	S<210>	4027.5	613	341	S<150>	1327.5	613
222	VCOM_PREC	5100	-603	282	S<209>	3982.5	613	342	S<149>	1282.5	613
223	VCOM_DC	5150	-603	283	S<208>	3937.5	613	343	S<148>	1237.5	613
224	VCOM_DC	5200	-603	284	S<207>	3892.5	613	344	S<147>	1192.5	613
225	VCOM_DC	5250	-603	285	S<206>	3847.5	613	345	S<146>	1147.5	613
226	VREFI	5300	-603	286	S<205>	3802.5	613	346	S<145>	1102.5	613
227	VREFO	5350	-603	287	S<204>	3757.5	613	347	S<144>	1057.5	613
228	RESETB	5400	-603	288	S<203>	3712.5	613	348	S<143>	1012.5	613
229	Contact_VSS3	5450	-603	289	S<202>	3667.5	613	349	S<142>	967.5	613
230	Contact_VSS3	5500	-603	290	S<201>	3622.5	613	350	S<141>	922.5	613
231	VCOM	5550	-603	291	S<200>	3577.5	613	351	S<140>	877.5	613
232	VCOM	5600	-603	292	S<199>	3532.5	613	352	S<139>	832.5	613
233	VCOM	5650	-603	293	S<198>	3487.5	613	353	S<138>	787.5	613
234	VCOM	5700	-603	294	S<197>	3442.5	613	354	S<137>	742.5	613
235	VCOM	5750	-603	295	S<196>	3397.5	613	355	S<136>	697.5	613
236	VCOM	5800	-603	296	S<195>	3352.5	613	356	S<135>	652.5	613
237	VCOM	5850	-603	297	S<194>	3307.5	613	357	S<134>	607.5	613
238	DUMMY<8>	5900	-603	298	S<193>	3262.5	613	358	S<133>	562.5	613
239	DUMMY<9>	5950	-603	299	S<192>	3217.5	613	359	S<132>	517.5	613
240	DUMMY<11>	5872.5	613	300	S<191>	3172.5	613	360	S<131>	472.5	613

No	PAD Name	X	Y	No	PAD Name	X	Y	No	PAD Name	X	Y
361	S<130>	427.5	613	411	S<80>	-1822.5	613	461	S<30>	-4072.5	613
362	S<129>	382.5	613	412	S<79>	-1867.5	613	462	S<29>	-4117.5	613
363	S<128>	337.5	613	413	S<78>	-1912.5	613	463	S<28>	-4162.5	613
364	S<127>	292.5	613	414	S<77>	-1957.5	613	464	S<27>	-4207.5	613
365	S<126>	247.5	613	415	S<76>	-2002.5	613	465	S<26>	-4252.5	613
366	S<125>	202.5	613	416	S<75>	-2047.5	613	466	S<25>	-4297.5	613
367	S<124>	157.5	613	417	S<74>	-2092.5	613	467	S<24>	-4342.5	613
368	S<123>	112.5	613	418	S<73>	-2137.5	613	468	S<23>	-4387.5	613
369	S<122>	67.5	613	419	S<72>	-2182.5	613	469	S<22>	-4432.5	613
370	S<121>	22.5	613	420	S<71>	-2227.5	613	470	S<21>	-4477.5	613
371	S<120>	-22.5	613	421	S<70>	-2272.5	613	471	S<20>	-4522.5	613
372	S<119>	-67.5	613	422	S<69>	-2317.5	613	472	S<19>	-4567.5	613
373	S<118>	-112.5	613	423	S<68>	-2362.5	613	473	S<18>	-4612.5	613
374	S<117>	-157.5	613	424	S<67>	-2407.5	613	474	S<17>	-4657.5	613
375	S<116>	-202.5	613	425	S<66>	-2452.5	613	475	S<16>	-4702.5	613
376	S<115>	-247.5	613	426	S<65>	-2497.5	613	476	S<15>	-4747.5	613
377	S<114>	-292.5	613	427	S<64>	-2542.5	613	477	S<14>	-4792.5	613
378	S<113>	-337.5	613	428	S<63>	-2587.5	613	478	S<13>	-4837.5	613
379	S<112>	-382.5	613	429	S<62>	-2632.5	613	479	S<12>	-4882.5	613
380	S<111>	-427.5	613	430	S<61>	-2677.5	613	480	S<11>	-4927.5	613
381	S<110>	-472.5	613	431	S<60>	-2722.5	613	481	S<10>	-4972.5	613
382	S<109>	-517.5	613	432	S<59>	-2767.5	613	482	S<9>	-5017.5	613
383	S<108>	-562.5	613	433	S<58>	-2812.5	613	483	S<8>	-5062.5	613
384	S<107>	-607.5	613	434	S<57>	-2857.5	613	484	S<7>	-5107.5	613
385	S<106>	-652.5	613	435	S<56>	-2902.5	613	485	S<6>	-5152.5	613
386	S<105>	-697.5	613	436	S<55>	-2947.5	613	486	S<5>	-5197.5	613
387	S<104>	-742.5	613	437	S<54>	-2992.5	613	487	S<4>	-5242.5	613
388	S<103>	-787.5	613	438	S<53>	-3037.5	613	488	S<3>	-5287.5	613
389	S<102>	-832.5	613	439	S<52>	-3082.5	613	489	S<2>	-5332.5	613
390	S<101>	-877.5	613	440	S<51>	-3127.5	613	490	S<1>	-5377.5	613
391	S<100>	-922.5	613	441	S<50>	-3172.5	613	491	S<0>	-5422.5	613
392	S<99>	-967.5	613	442	S<49>	-3217.5	613	492	RSWB	-5467.5	613
393	S<98>	-1012.5	613	443	S<48>	-3262.5	613	493	GSWB	-5512.5	613
394	S<97>	-1057.5	613	444	S<47>	-3307.5	613	494	BSWB	-5557.5	613
395	S<96>	-1102.5	613	445	S<46>	-3352.5	613	495	L_GCLK4B	-5602.5	613
396	S<95>	-1147.5	613	446	S<45>	-3397.5	613	496	L_GCLK3B	-5647.5	613
397	S<94>	-1192.5	613	447	S<44>	-3442.5	613	497	L_GCLK2B	-5692.5	613
398	S<93>	-1237.5	613	448	S<43>	-3487.5	613	498	L_GCLK1B	-5737.5	613
399	S<92>	-1282.5	613	449	S<42>	-3532.5	613	499	L_GSPB	-5782.5	613
400	S<91>	-1327.5	613	450	S<41>	-3577.5	613	500	DUMMY<15>	-5827.5	613
401	S<90>	-1372.5	613	451	S<40>	-3622.5	613	501	DUMMY<16>	-5872.5	613
402	S<89>	-1417.5	613	452	S<39>	-3667.5	613				
403	S<88>	-1462.5	613	453	S<38>	-3712.5	613				
404	S<87>	-1507.5	613	454	S<37>	-3757.5	613				
405	S<86>	-1552.5	613	455	S<36>	-3802.5	613				
406	S<85>	-1597.5	613	456	S<35>	-3847.5	613				
407	S<84>	-1642.5	613	457	S<34>	-3892.5	613				
408	S<83>	-1687.5	613	458	S<33>	-3937.5	613				
409	S<82>	-1732.5	613	459	S<32>	-3982.5	613				
410	S<81>	-1777.5	613	460	S<31>	-4027.5	613				

4.DISPLAY PIN DESCRIPTION

4.1 POWER SUPPLY PINS

Table 4.1.1 Power Supply Pins

Symbol	I/O	Description
VDD3	I Power	I/O power supply for external interface. (VDD3: +1.65 ~ +3.3 V)
AVDD	O Power	A power output pin for source driver block that is generated from power block. Connect a capacitor for stabilization. (AVDD: +3.4 ~ +6.0 V)
GVDD	O Power	A standard level for grayscale voltage generator. Connect a capacitor for stabilization. When internal GVDD generator is not used, connect an external power supply. (GVDD = 3.0 ~ 5.0V & AVDD – 0.5 V)
VCI	I Power	Analog power supply (VCI : 2.5 ~ 3.3V)
VCI_REF	I Power	A Reference voltage for VCI. Must connect to VCI at FPC
VCI_MDDI	I Power	Analog power supply (VCI_MDDI : 2.5 ~ 3.3V)
VSS	I Power	System ground. (0V)
VSS3	I Power	System ground level for I/O.
VSS_MDDI	I Power	System ground level for MDDI Block
VSSC	I Power	System ground level for step up circuit block.
MTP_EP	I Power	Power supply for Non-volatile Memory. (21.5± 0.5V) If MTP is not used, this pad should be floated.
MTP_PP	I Power	Power supply for Non-volatile Memory (17.5± 0.5V) If MTP is not used, this pad should be floated.
AVSS	I Power	System ground level for source driver block.
VGS	I Power	Gamma ground level.

Table 4.1.2 Power Supply Pins (continued)

Symbol	I/O	Description
VCI1	O Power	A reference voltage in step-up circuit 1. Connect a capacitor for stabilization. VCI1 can not exceed 3 V.
VREFO	O	A reference voltage for GVDD, VCOMH, VCOML. (External Short to VREFI)
VREFI	I	A reference voltage for GVDD, VCOMH, VCOML.
VCOMPREC	O	When the coupling mode is driven, this pin is used. Connect to VCOM.
VCOM	O	Outputs the square wave signal obtained through common modulation of Vp-p. - R16H : COMA is low, VCOM = VCOMH – AVSS - R16H : COMA is high, VCOM = VCOMH – VCOML
VCOMDC	O	When the coupling mode is driven, this pin is used for the common center voltage.
VCOMR	I/O	A reference voltage of VCOMH. When VCOMH is externally adjusted, halt the internal adjuster of VCOMH by setting the register and inserting a variable resistor between GVDD and VSS. When this pin is not externally adjusted, leave it open and adjust VCOMH by setting the internal register.
VCOMH	O	This pin indicates a high level of VCOM that is generated from driving the VCOM alternation. Connect this pin to the capacitor for stabilization.
VCOML	O	When the VCOM alternation is driven, this pin indicates a low level of VCOM. An internal register can be used to adjust the voltage. Connect this pin to a capacitor for stabilization, and be careful of the polarity of capacitor for available voltage. (0 ~ 1.0V)
VGH	O Power	This pin is a positive power output pin for gate driver, internal step-up circuits, bias circuits, and operational amplifiers. Connect a capacitor for stabilization. Range : 7.5 V ~ 16.0 V. External Cap. 2.2uF.
VGL	O Power	VGL is VGLROUT regulator power voltage. To protect IC against Latch up, connect the cathode of the schottky diode to the VSS pad. And the anode of the schottky diode to the VGL pad. Refer to the application circuit. Connect a capacitor for stabilization. Range : -11.0V ~ -5.5V. External Cap. 1.0uF.
VGLROUT	O Power	VGLROUT voltage is gate negative voltage. VGLROUT is generated by regulator amp. VGLRC register is VGLROUT level control. Range : -10.5V ~ -5.0V
VR1	O Power	VR1 voltage is VGH, VGL reference voltage Range : 2.0V ~ 5.0V
VR2	O Power	VR2 voltage is VGH reference voltage Range : 2.0V ~ 5.0V
EX_CLK	I/O	In Input mode, it will be used as Test Pin [581KHz ~ 1730KHz frequency] In Output mode, leave this pin open. Used to analyze the internal oscillation frequency.
C11M,C11P C12M,C12P	-	Connect the step-up capacitor for generating the AVDD level. C12M & C12P can be used as an option only for high current consumption.
C21M,C21P C22M,C22P	-	Connect a step-up capacitor for generating the VGH, VGL level.

4.2 HOST/EXTERNAL INTERFACE PINS

Table 4.2.1 Host Interface Pins

Symbol	I/O	Description
IM[3:0]	I	System interface selection pins.
CSB	I	Chip selection pin, active low.
RS	I	Data / Command selection pin. When parallel data transfer has been selected, this pin is used to distinguish between data from memory and commands. Low: indicates that data (DB bus) is commands, High: indicates that data (DB bus) is display data.
RW_WRB	I	68-system I/F: Read/Write select signal Low(write), High(read) 80-system I/F: Write strobe signal. Active low. Selecting RGB mode, it is used as SCL.
E_RDB	I	68-system I/F: Strobe signal. Active high. 80-system I/F: Read strobe signal. Active low Selecting RGB mode, it is used as SDI.
DB[17:0]	I/O	Data bus pins. Unused pins are fixed to VSS3.
RESETB	I	External reset pin. Active low. Initializes the IC, when this signal is low. Must be reset after the power is stable. **NOTE:** These three pins are connected together inside the chip. So when one is used as a reset pin, the other one should be left floating.
ENABLE	I	Data enable pin in RGB I/F mode. If not used, please fix this pin at VSS3 level.
VSYNC	I	Vertical synchronous pin in RGB I/F mode. If not used, please fix this pin at VSS3 level.
HSYNC	I	Horizontal synchronous pin in RGB I/F mode. If not used, please fix this pin at VSS3 level.
DOTCLK	I	Data clock pin in RGB I/F mode. If not used, please fix this pin at VSS3 level.
PD[17:0]	I/O	RGB data input bus. 18-bit interface: PD 17-0 16-bit interface: PD 17-13, PD 11-1 6-bit interface: PD 17-12 In the MDDI mode, these pins are used for data bus of Sub Panel driver IC.

Table 4.2.2 MDDI Interface Pins

Symbol	I/O	Description
MDP	I/O	Positive MDDI data pin. If MDDI is not used, this pad should be floating.
MDN	I/O	Negative MDDI data pin. If MDDI is not used, this pad should be floating.
MSP	I	Positive MDDI strobe pin. If MDDI is not used, this pad should be floating.
MSN	I	Negative MDDI strobe pin. If MDDI is not used, this pad should be floating.
DB[17:13] (not used)	O	In MDDI mode, these pins should be floating.
GPIO[9:0] (DB[12:3])	I/O	General purpose input/output pins. If GPIO is not used in MDDI mode, this pin should be fixed to VSS3.
S_CSB (DB[2])	O	Chip select for Sub Panel Driver IC. Low: Sub Panel Driver IC is selected and can be accessed. High: Sub Panel Driver IC is not selected and can not be accessed. If sub panel is not used in MDDI mode, this pin should be floating
S_RS (DB[1])	O	Register select for Sub Panel Driver IC. Low : Index/status, High : Control Must be fixed at VSS level, when this signal is not used. If sub panel is not used in MDDI mode, this pin should be floating
S_WRB (DB[0])	O	Write Strobe signal for Sub Panel Driver IC. Only 80-system 18/16 bit mode is enabled, so Data is fetched at the rising edge. If sub panel is not used in MDDI mode, this pin should be floating
S_DB17-0 (PD[17:0])	O	For Sub Panel, this pin can be used to transfer DB [17:0] data to Sub Panel Driver IC. If sub panel is not used in MDDI mode, this pin should be floating.
HSYNC VSYNC ENABLE DOTCLK	I	In MDDI mode, fixed it to VSS3.
RW_WRB E_RDB RS	I	In MDDI mode, fixed it to VSS3.
CSB	I	In MDDI mode, fixed it to VDD3.

NOTE : In MDDI mode, MDP(MSP), MDN(MSN) ports should be terminated with 100Ω resister

4.3 DRIVER OUTPUT PINS

Table 4.3.1 Source Output Pins

Symbol	I/O	Description
S1 to S240	O	Source driver output pins.

Table 4.3.2 Gate Driver Control Pins

Symbol	I/O	Description
LGSPB	O	STB output (Even: Left side). This pin is a gate start pulse signal. Amplitude: VGH-VGLROUT
LGCLK1B	O	CLK 1 output (Even: Left side). This pin is a gate clock signal. Amplitude: VGH-VGLROUT
LGCLK2B	O	CLK 2 output (Even: Left side). This pin is a gate clock signal. Amplitude: VGH-VGLROUT
LGCLK3B	O	CLK 3 output (Even: Left side). This pin is a gate clock signal. Amplitude: VGH-VGLROUT
LGCLK4B	O	CLK 4 output (Even: Left side). This pin is a gate clock signal. Amplitude: VGH-VGLROUT
RGSPB	O	STB output (Odd: Right side). This pin is a gate start pulse signal. Amplitude: VGH-VGLROUT
RGCLK1B	O	CLK 1 output (Odd: Right side). This pin is a gate clock signal. Amplitude: VGH-VGLROUT
RGCLK2B	O	CLK 2 output (Odd: Right side). This pin is a gate clock signal. Amplitude: VGH-VGLROUT
RGCLK3B	O	CLK 3 output (Odd: Right side). This pin is a gate clock signal. Amplitude: VGH-VGLROUT
RGCLK4B	O	CLK 4 output (Odd: Right side). This pin is a gate clock signal. Amplitude: VGH-VGLROUT

Table 4.3.3 RGB Switch Control Pins

Symbol	I/O	Description
RSWB	O	This pin is panel of multi-plectra control signal. <R> select signal. Signal is outputted to the timing set as R72h and R75h. Amplitude: VGH-VGLROUT
GSWB	O	This pin is panel of multi-plectra control signal. <G> select signal. Signal is outputted to the timing set as R73h and R76h. Amplitude: VGH-VGLROUT
BSWB	O	This pin is panel of multi-plectra control signal. <B> select signal. Signal is outputted to the timing set as R74h and R7h7. Amplitude: VGH-VGLROUT

4.4 MISCELLANEOUS PINS

Table 4.4.1 Miscellaneous Pins

Symbol	I/O	Description
TEST_MODE0 TEST_MODE2	I	Input pins for test. In normal operation, connect this pin to VSS3.
TEST_MODE1	I	Input pin for test. In normal operation, connect this pin to VSS3 In RGB I/O sharing mode, this pin should be fixed to VDD3.
DISPTMG/M/ CL1/FLM/ TSO1/ TSO0 /PREC/EQ	O	Output pins for test. In normal operation, leave this pin open.
DUMMY	-	Dummy pin. Open or connect VSS3.
S0, S241	O	Source driver output pins. (S0 = S1, S241 = 240)

4.5 INTERFACE PIN CONFIGURATION

Table 4.5.1 Source Output Pins

PIN NAME	68 System				80 System				RGB (*Note1)		MDDI mode
	18bit	16bit	9bit	8bit	18bit	16bit	9bit	8bit	Normal	I/O sharing	MDDI
IM[0]	0	0	1	1	0	0	1	1	ID	ID	0
IM[1]	0	0	0	0	1	1	1	1	0	0	0
IM[2]	0	0	0	0	0	0	0	0	1	1	1
IM[3]	1	0	1	0	1	0	1	0	0	0	1
MDP	floating	floating	floating	floating	floating	floating	floating	floating	floating	floating	MDP
MDN	floating	floating	floating	floating	floating	floating	floating	floating	floating	floating	MDN
MSP	floating	floating	floating	floating	floating	floating	floating	floating	floating	floating	MSP
MSN	floating	floating	floating	floating	floating	floating	floating	floating	floating	floating	MSN
DB[17:13]	DB[17:13]	DB[17:13]	DB[17:13]	DB[17:13]	DB[17:13]	DB[17:13]	DB[17:13]	DB[17:13]	VSS3	PD[17:13]	floating
DB[12:10]	DB[12:10]	DB[12:10]	DB[12:10]	DB[12:10]	DB[12:10]	DB[12:10]	DB[12:10]	DB[12:10]	VSS3	PD[12:10]	GPIO[9:7]
DB[9]	DB[9]	floating	DB[9]	floating	DB[9]	floating	DB[9]	floating	VSS3	PD[9]	GPIO[6]
DB[8:3]	DB[8:3]	DB[8:3]	floating	floating	DB[8:3]	DB[8:1]	floating	floating	VSS3	PD[8:3]	GPIO[5:0]
DB[2]	DB[2]	DB[2]	floating	floating	DB[2]	DB[2]	floating	floating	VSS3	PD[2]	S_CSB
DB[1]	DB[1]	DB[1]	floating	floating	DB[1]	DB[1]	floating	floating	VSS3	PD[1]	S_RS
DB[0]	DB[0]	floating	floating	floating	DB[0]	VDD3	floating	floating	VSS3	PD[0]	S_WRB
PD[17:0]	floating	floating	floating	floating	floating	floating	floating	floating	PD[17:0]	floating	S_DB(*Note2)
CSB	CSB	CSB	CSB	CSB	CSB	CSB	CSB	CSB	CSB	CSB	VDD3
RW_WRB	RW	RW	RW	RW	WRB	WRB	WRB	WRB	SCL	SCL	VSS3
E_RDB	E	E	E	E	RDB	RDB	RDB	RDB	SDI	SDI	VSS3
RS	RS	RS	RS	RS	RS	RS	RS	RS	VSS3	VSS3	VSS3
VSYNC	VSS3	VSS3	VSS3	VSS3	VSS3	VSS3	VSS3	VSS3	VSYNC	VSYNC	VSS3
HSYNC	VSS3	VSS3	VSS3	VSS3	VSS3	VSS3	VSS3	VSS3	HSYNC	HSYNC	VSS3
DOTCLK	VSS3	VSS3	VSS3	VSS3	VSS3	VSS3	VSS3	VSS3	DOTCLK	DOTCLK	VSS3
ENABLE	VSS3	VSS3	VSS3	VSS3	VSS3	VSS3	VSS3	VSS3	ENABLE	ENABLE	VSS3
TEST_MODE[2]	0	0	0	0	0	0	0	0	0	0	0
TEST_MODE[1]	0	0	0	0	0	0	0	0	0	1	0
TEST_MODE[0]	0	0	0	0	0	0	0	0	0	0	0
TSO[0]	floating	floating	floating	floating	floating	floating	floating	floating	SDO	SDO	floating
PREC	floating	floating	floating	floating	floating	floating	floating	floating	floating	floating	floating
EQ	floating	floating	floating	floating	floating	floating	floating	floating	floating	floating	floating
M	floating	floating	floating	floating	floating	floating	floating	floating	floating	floating	floating

[NOTES]

Interface	Description	Remark
RGB	18bit I/F : PD[17:0] 16bit I/F : PD[17:13], PD[11:1] 6bit I/F : PD[17:12]	Unused Pins are not fixed any value, because of floating state which is defined output pins
MDDI	PD[17:0] : S_DB[17:0]	PD [17:0] is defined as output. These pins are for sub panel DDI control signals For details, See “SUB PANEL DDI CONTROL” section.

Using for RGB I/O sharing mode, TEST_MODE [2:0] must be fixed to “3’b010”
All unused input pins except for MDDI LDVS and CSB pins must be fixed to VSS3.

5. FUNCTIONAL DESCRIPTION

5.1 SYSTEM INTERFACE

S6D1121 has twelve high-speed system interfaces: 80-system 18/16/9/8bit CPU Interfaces, 68-system 18/16/9/8bit CPU Interfaces, two external display interface (RGB Interface, VSYNC interface), and two serial interfaces (SPI: Serial Peripheral Interface, MDDI: High Speed Serial Interface). The IM [3:0] pins determine the interface mode.

5.1.1 INTERFACE TYPE SELECTION

The selection of a given interfaces are done by setting IM [3:0] pins as show in ***Table 5.1.1.1.***

Table 5.1.1.1 System Interface Type Selection and DB Pins Assignment

IM3	IM2	IM1	IM0/ID	MPU interface mode	DB PIN assign
VSS	VSS	VSS	VSS	68-system 16-bit bus interface	DB17-10, DB8-1
VSS	VSS	VSS	VDD3	68-system 8-bit bus interface	DB17-10
VSS	VSS	VDD3	VSS	80-system 16-bit bus interface	DB17-10, DB8-1
VSS	VSS	VDD3	VDD3	80-system 8-bit bus interface	DB17-10
VSS	VDD3	VSS	ID	Serial peripheral interface (SPI)	E_RDB,TSO[0] (SDI, SDO)
VSS	VDD3	VDD3	*	Non-selecting	-
VDD3	VSS	VSS	VSS	68-system 18-bit bus interface	DB17-0
VDD3	VSS	VSS	VDD3	68-system 9-bit bus interface	DB17-9
VDD3	VSS	VDD3	VSS	80-system 18-bit bus interface	DB17-0
VDD3	VSS	VDD3	VDD3	80-system 9-bit bus interface	DB17-9
VDD3	VDD3	VSS	*	MDDI interface	-
When a SPI mode is selected, the IM0 pin is used as ID setting bit for a device code. The other cases above, setting prohibited.					

By setting the TEST_MODE pins, PD bus can reduce as shown in ***Table 5.1.1.2.***

Table 5.1.1.2 RGB Interface Type Selection and DB/PD Pins Assignment

TEST_MODE[2:0]			RGB interface mode	DB PIN assign
VSS	VDD3	VSS	18-bit parallel bus interface	DB17-0
			16-bit parallel bus interface	DB17-13, DB11-1
			6-bit parallel bus interface	DB17-12
VSS	VSS	VSS	18-bit parallel bus interface	PD17-0
			16-bit parallel bus interface	PD17-13, PD11-1
			6-bit parallel bus interface	PD17-12
In case of the I/O sharing DB bus and PD bus, the TEST_MODE pins must be fixed to “010”.				

5.1.2 REGISTER TYPE SELECTION

The S6D1121 has three 18-bit registers: an index register (IR), a write data register (WDR), and a read data register (RDR). The IR is a register to store index information from each control register. The WDR is a register that temporarily stores data to be written into each control register and GRAM. The RDR is a register to temporarily store data which is read from the GRAM. The data to be written to GRAM from MPU is once written to the WDR and then automatically written to GRAM by internal operation. Since the data is read from GRAM through the RDR, the data read out first is invalid and the data following that is read out normally.

Table 5.1.2.1 Register Selection (18-/16-/9-/8- Parallel Interface)

SYSTEM	RW_WRB	E_RDB	RS	Operations
68	0	1	0	Write index to IR
	1	1	0	Read internal status (Current Gate Line Status)
	0	1	1	Write to control register and GRAM through WDR
	1	1	1	Read from GRAM and control register through RDR
80	0	1	0	Write index to IR
	1	0	0	Read internal status (Current Gate Line Status)
	0	1	1	Write to control register and GRAM through WDR
	1	0	1	Read from GRAM and control register through RDR

Table 5.1.2.2 Register Selection (Serial Peripheral Interface)

R/W bit	RS bit	Operations
0	0	Write index to IR
1	0	Read internal status
0	1	Write data to control register and GRAM through WDR
1	1	Read data from GRAM and control register through RDR

5.1.3 DATA TRANSFER MODE SELECTION

When the 18-bit parallel interface is selected, the length of 1 pixel is fixed to 18 bits. With the 16-bit, 9-bit or 8-bit parallel interface, however, the length of 1 pixel can be selected from 18 or 16 bits.

If the 16-bit, 9-bit or 8-bit parallel interface is selected, therefore, several modes of transferring data to the display RAM are selectable. The mode is selected by using the TRI, DFM registers.

Table 5.1.3.1 Interface and Data Transfer Mode

TRI	DFM	Interface		Number of Data of 1 Pixel	Mode of Transferring 1-Pixel Data
0	0	68/80-system 18bit		18-bit	18-bit transfer
0	0	68/80-system 16bit		16-bit	16-bit transfer
0	0	68/80-system 9bit		18-bit	9-bit transfer twice
0	0	68/80-system 8bit		16-bit	8-bit transfer twice
1	0	80-system 16bit		18-bit	16-bit + 2-bit transfer
1	1	80-system 16bit		18-bit	2-bit + 16-bit transfer
1	0	80-system 8bit		18-bit	6bit transfer three times
1	1	80-system 8bit		16-bit	6bit transfer three times
X	X	RGB	18-bit	18-bit	18-bit transfer
X	X		16-bit	16-bit	16-bit transfer
X	X		6-bit	18-bit	6-bit transfer three times

Remark X: Don't care (H/L)

5.1.3.1 68/80 SYSTEM DATA TRANSFER MODE SELECTION

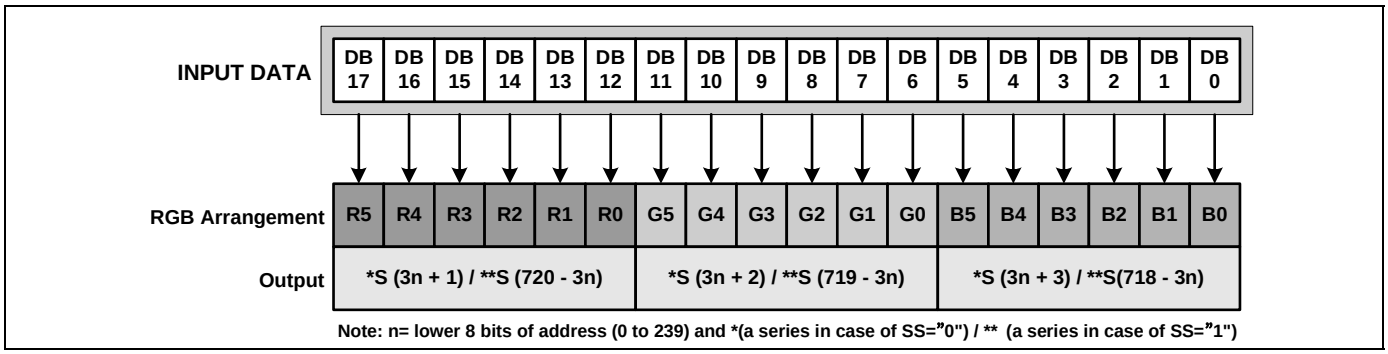


Figure 5.1.3.1.1 68/80-System 18-Bit Interface (TRI=0, DFM=0)

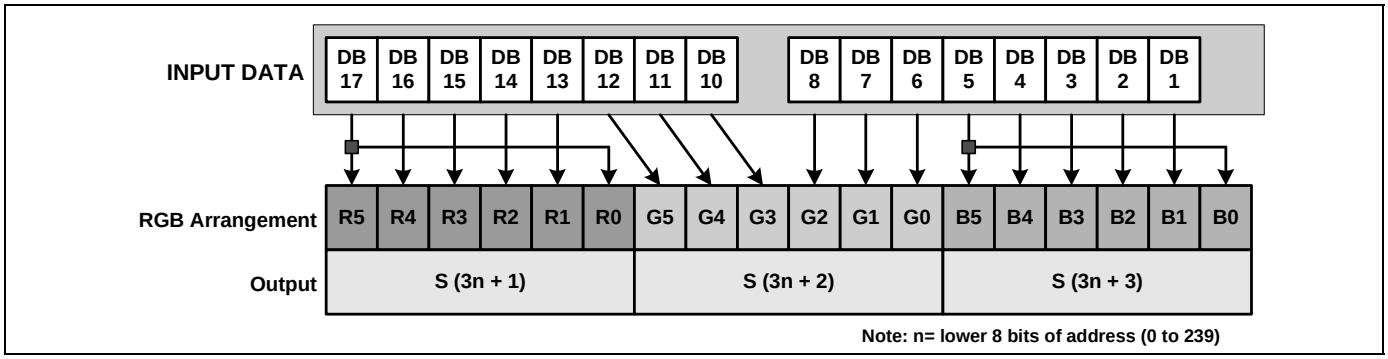


Figure 5.1.3.1.2 68/80-System 16-Bit Interface (TRI=0, DFM=0)

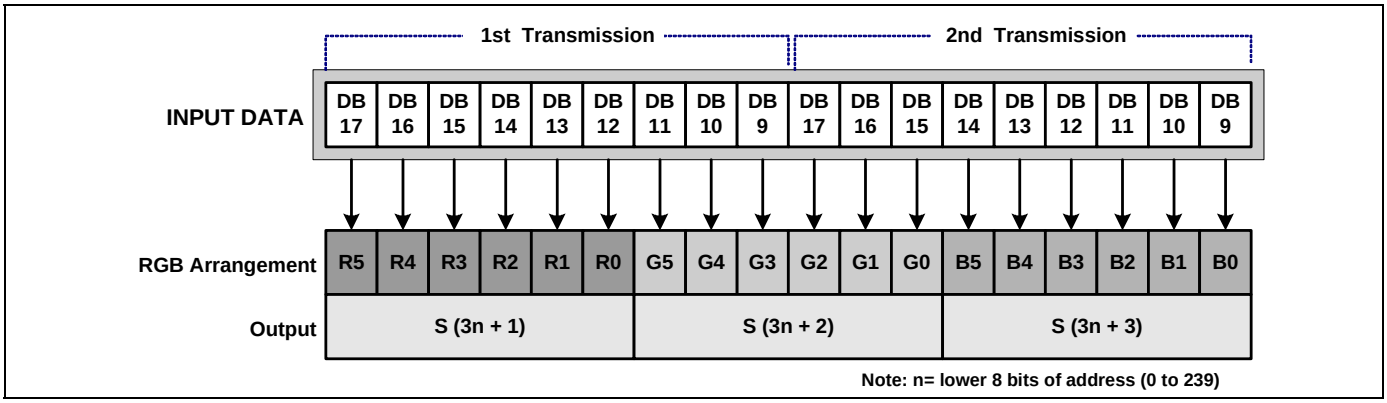


Figure 5.1.3.1.3 68/80-System 9-Bit Interface (TRI=0, DFM=0)

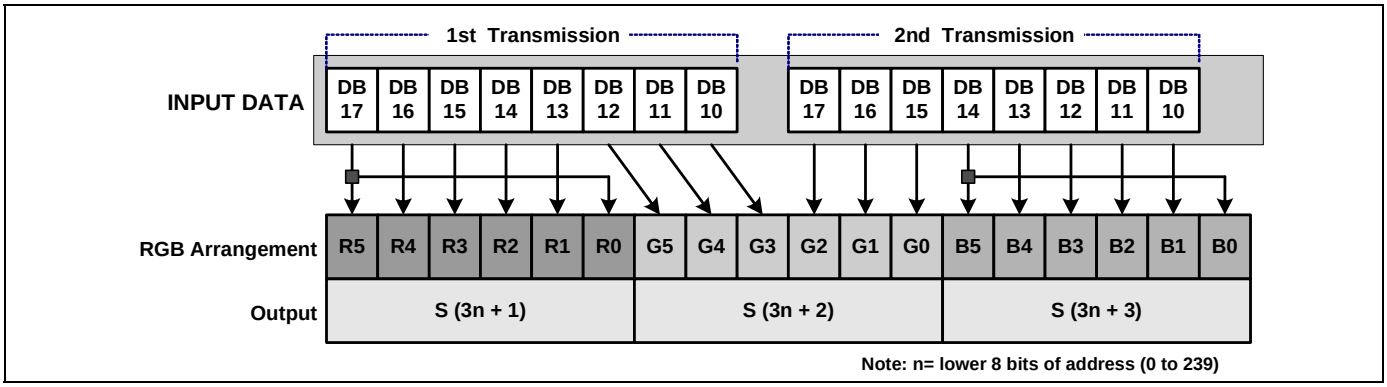


Figure 5.1.3.1.4 68/80-System 8-Bit Interface (TRI=0, DFM=0)

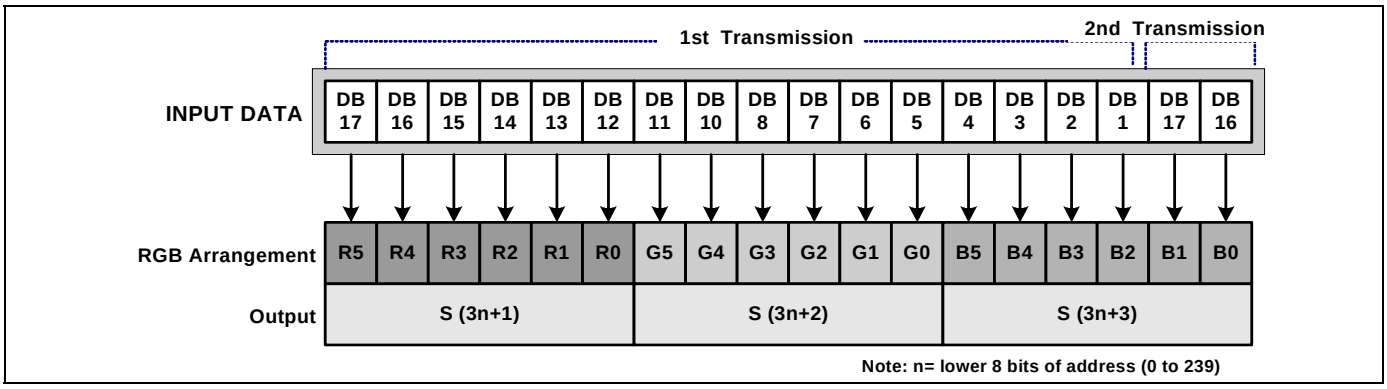


Figure 5.1.3.1.5 80-System 16-Bit Interface (TRI=1, DFM=0): 2 Times Transmission (262 K color)

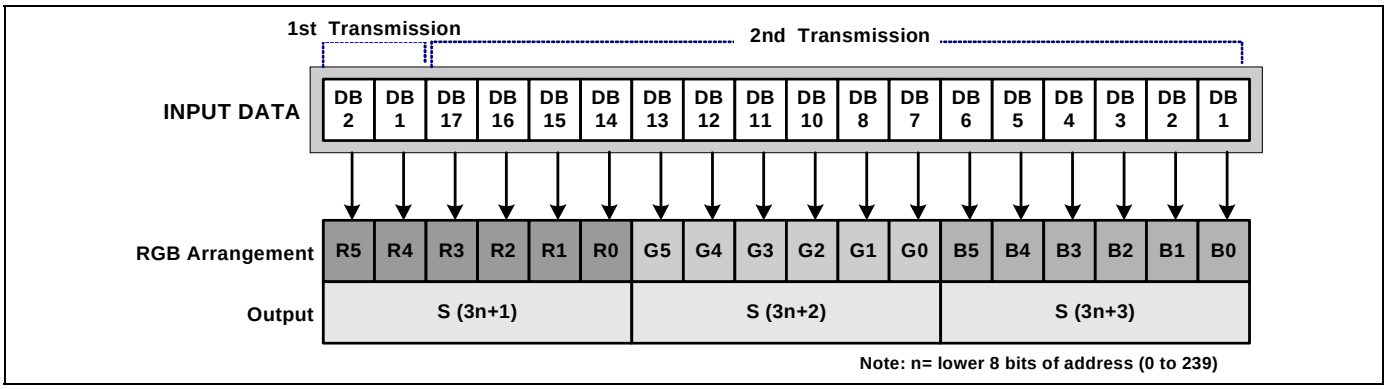


Figure 5.1.3.1.6 80-System 16-Bit Interface (TRI=1, DFM=1): 2 Times Transmission (262 K color)

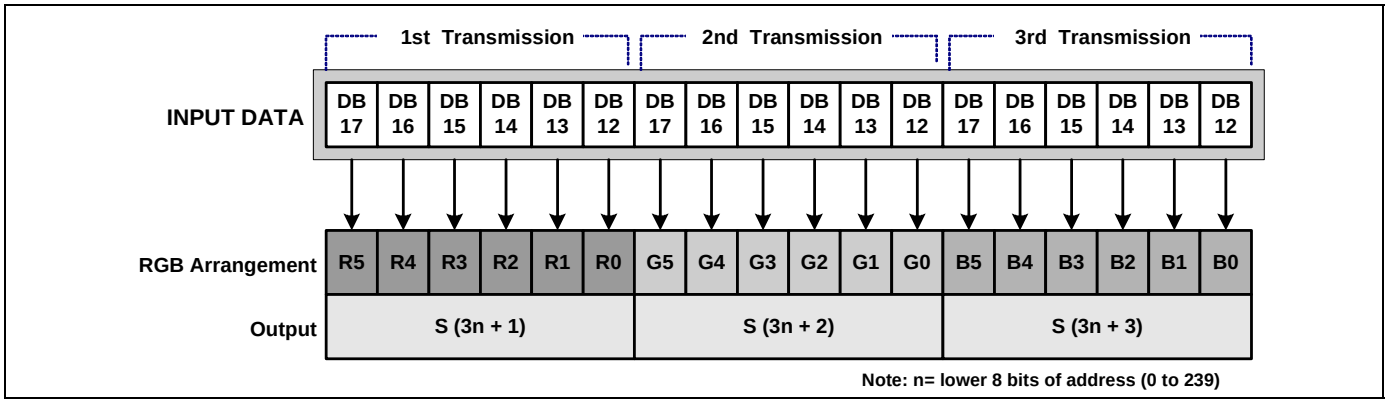


Figure 5.1.3.1.7 80-System 8-Bit Interface (TRI=1, DFM=0): 3 Times Transmission (262 K color)

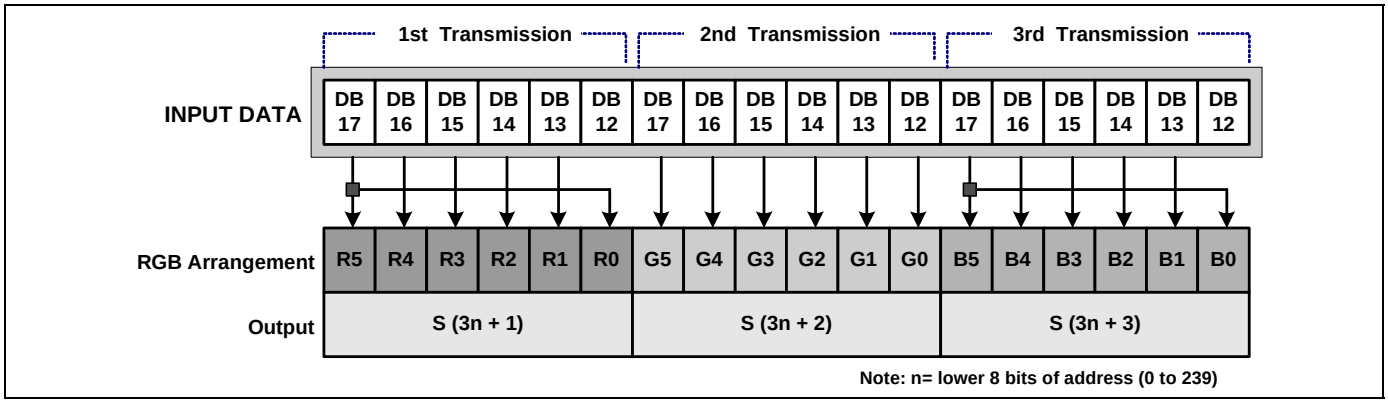


Figure 5.1.3.1.8 80-System 8-Bit Interface (TRI=1, DFM=1): 3 Times Transmission (65 K color)

5.1.3.2 RGB DATA TRANSFER MODE SELECTION

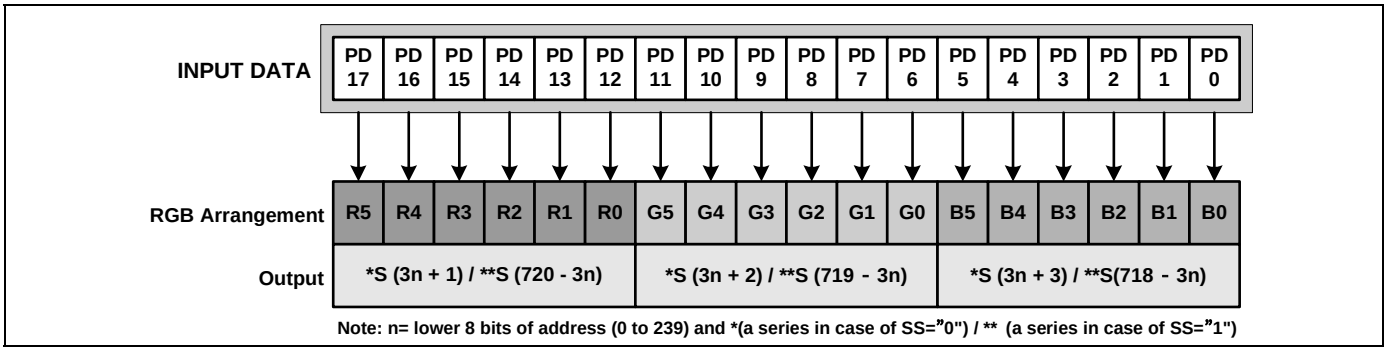


Figure 5.1.3.2.1 RGB-System 18-Bit Interface

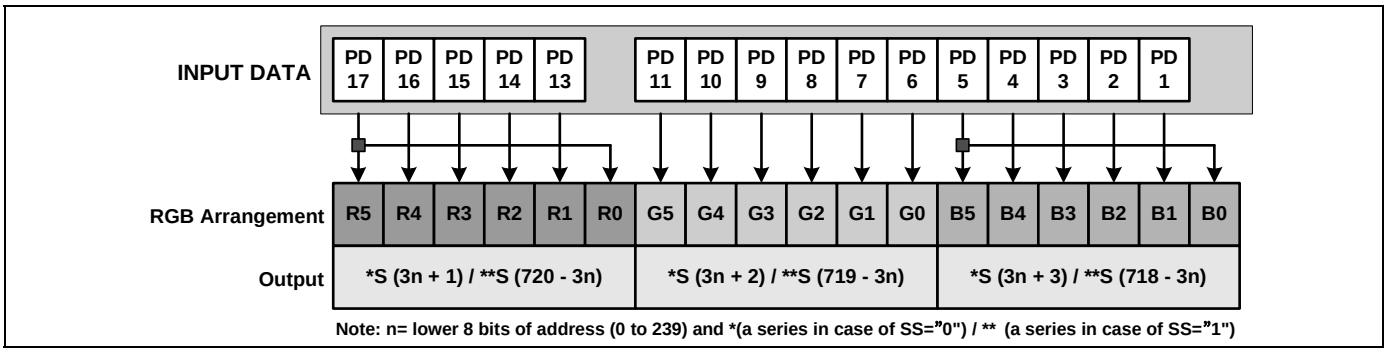


Figure 5.1.3.2.2 RGB-System 16-Bit Interface

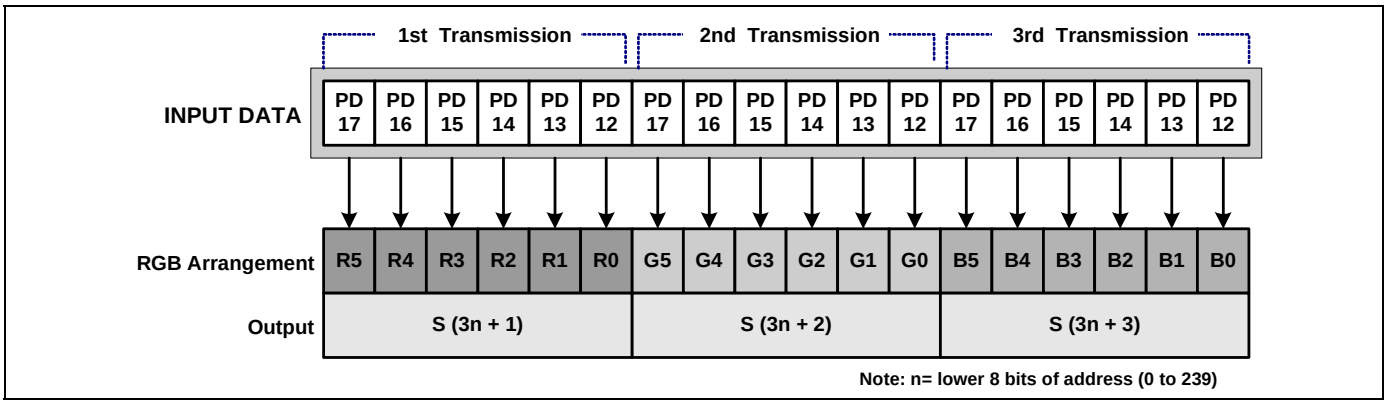


Figure 5.1.3.2.3 RGB-System 6-Bit Interface

5.1.3.3 COMMAND TRANSFER MODE SELECTION

The Transfer Type differs according to the 18-/16-/9-/8-bit interface.

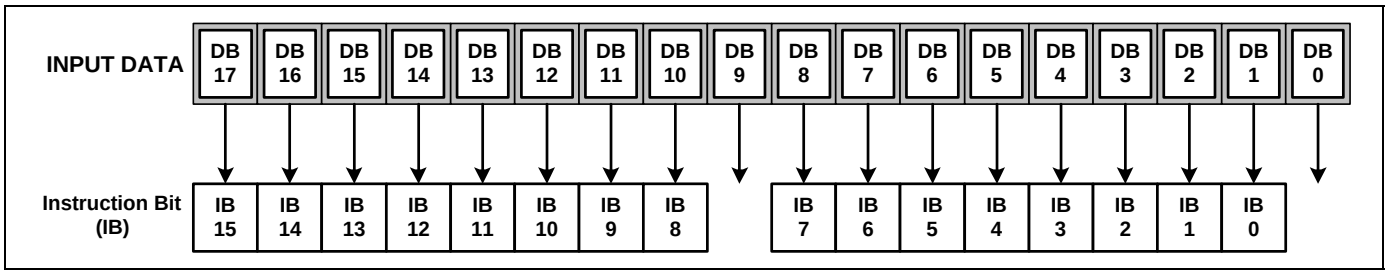


Figure 5.1.3.3.1 68/80-system 18-bit Interface

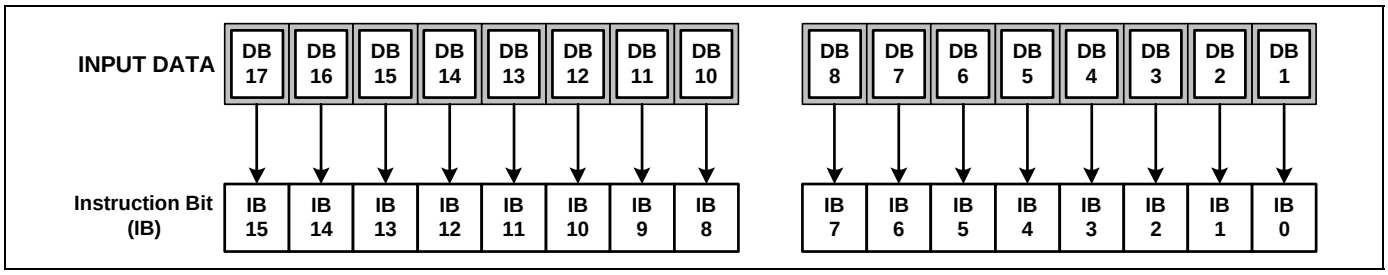


Figure 5.1.3.3.2 68/80-system 16-bit Interface

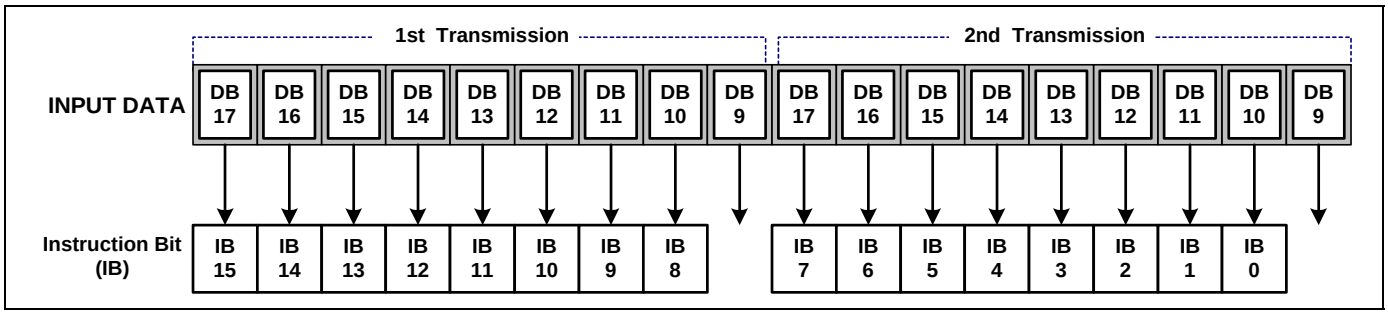


Figure 5.1.3.2.3 68/80-system 9-bit Interface

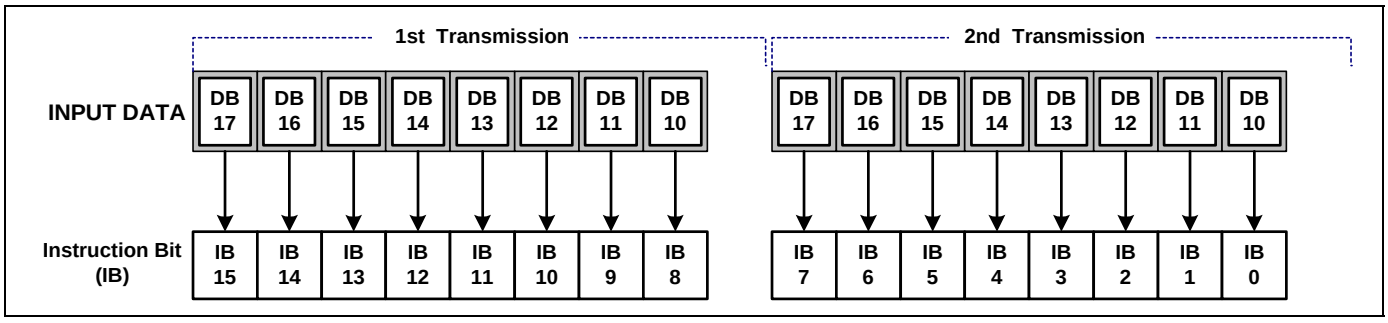


Figure 5.1.3.2.4 68/80-system 8-bit Interface

5.2 INTERFACE SPECIFICATION

The S6D1121 incorporates a system interface, which is used to set instructions, and two external display interfaces, which are used to display motion pictures. Selecting these interfaces to match the screen data (motion picture or still picture) enables efficient transfer of data for display.

5.2.1 DISPLAY OPERATION MODE

The external display interfaces include RGB interface and VSYNC interface. This allows flicker-free screen update. When RGB interface is selected, the synchronization signals (VSYNC, HSYNC, and DOTCLK) are available for use in operating the display. The data for display (PD17-0) is written according to the values of the data enable signal (ENABLE) in synchronization with the VSYNC, HSYNC, and DOTCLK signals. In addition, using the window address function enables rewriting only to the internal RAM area to display motion pictures. Using this function also enables simultaneously display of the motion picture area and the RAM data that was written.

The internal display operation is synchronized with the frame synchronization signal (VSYNC) in VSYNC interface mode. When writing to the internal RAM is done within the required time after the falling edge of VSYNC, motion pictures can be displayed via the conventional interface. There are some limitations on the timing and methods of writing to RAM.

The S6D1121 has four operation modes for each display state. These settings are specified by control instructions for external display interface. Transitions between modes should follow the transition flow.

Table 5.2.1.1 Display Operation Mode, RAM Access Selection and Display Operation Synchronization

Operation Mode	RAM Access Selection (RM)	Display Operation Mode (DM1-0)	Display Operation Synchronization
Internal Clock Operation (Displaying still picture)	System interface (RM=0)	Internal clock operation (DM1-0=00)	OSC
RGB interface (Displaying motion pictures)	RGB interface (RM=1)	RGB interface (DM1-0=01)	VSYNC, HSYNC, DOTCLK
VSYNC interface (Displaying motion pictures)	System interface (DM1-0=10)	VSYNC interface (RM=0)	OSC
MDDI interface (Displaying motion Pictures)	System interface (RM=0)	MDDI interface (DM1-0=00,10)	OSC

NOTES: 1) Instruction registers can only be set via system interface.
2) Switching among RGB and VSYNC interface cannot be done.
3) RGB interface and MDDI interface cannot be used at the same time.
4) RGB interface mode cannot be set during operations.
5) For mode transitions, see the section on the RGB display interface.

5.2.2 6800/80 SYSTEM INTERFACE

5.2.2.1 80-SERIES PARALLEL INTERFACE

The MCU uses a 12-wires 8-data parallel interface or 13-wires 9-data parallel interface or 20-wires 16-data parallel interface or 22-wires 18-data parallel interface. The chip-select CSB (active low) enables and disables the parallel interface. RESETB (active low) is an external reset signal. RW_WRB is the parallel data write, E_RDB is the parallel data read and DB [17:0] is parallel data.

The Graphics Controller Chip reads the data at the rising edge of RW_WRB signal. The RS of an external signal is the data/command flag. When RS='1', DB [17:0] bits are index parameters or display RAM data. When RS ='0', D [17:0] bits are index command. The 80-series bi-directional interface can be used for communication between the micro controller and LCD driver chip.

Write cycle sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (RW_WRB high-low-high sequence) consists of 3 controls (RS, E_RDB, RW_WRB_WRB) and data signals (DB [17:0]). RS is a control signal, which tells if the data is an index command or a data.

Read Cycle Sequence

The read cycle (E_RDB high-low-high sequence) means that the host reads information from display via interface. The display sends data (DB [17:0]) to the host when there is a falling edge of E_RDB and the host reads data when there is a rising edge of E_RDB.

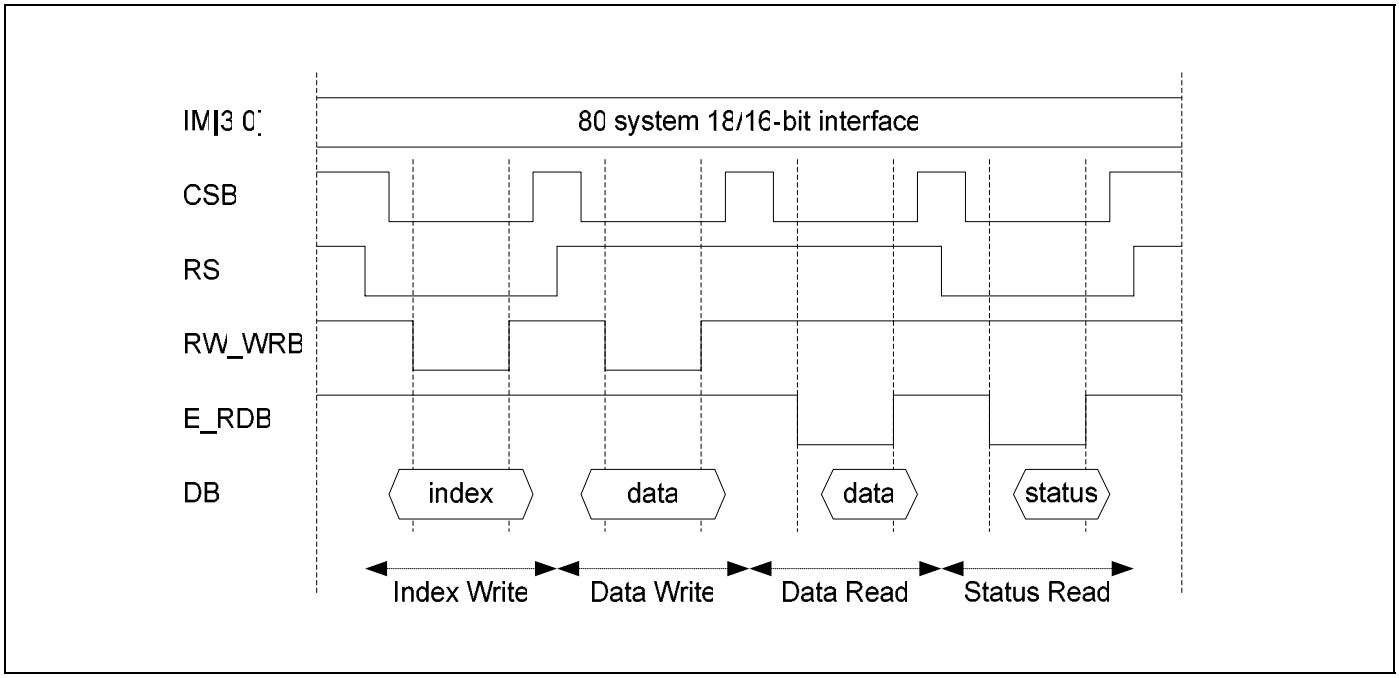


Figure 5.2.2.1.1 80-Series Interface Data Bus Status (data read and write)

5.2.2.2 6800-SERIES PARALLEL INTERFACE

The MCU uses a 12-wires 8-data parallel interface or 13-wires 9-data parallel interface or 20-wires 16-data parallel interface or 22-wires 18-data parallel interface. The chip-select CSB (active low) enables and disables the parallel interface. RESETB (active low) is an external reset signal. The E_RDB is the Read/Write flag and DB [17:0] is parallel data.

The Graphics Controller Chip reads the data at the falling edge of E_RDB signal when RW_WRB = '1' and writes the data at the falling of the E_RDB signal when RW_WRB ='0'. The RS is the data/command flag. When RS ='1', DB [17:0] bits are display RAM data. When RS = '0', DB [17:0] bits are index command.

The 6800-series bi-directional interface can be used for communication between the micro controller and LCD driver chip.

Write cycle sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (E_RDB low-high-low sequence) consists of 3 control signals (RS, E_RDB, RW_WRB) and data signals (DB [17:0]). RS is a control signal, which tells if the data is a index command or a data.

Read cycle sequence

The read cycle (E_RDB high-low-high sequence) means that the host reads information from display via interface. The display sends data (DB [17:0]) to the host when there is a falling edge of E_RDB and the host reads data when there is a rising edge of E_RDB.

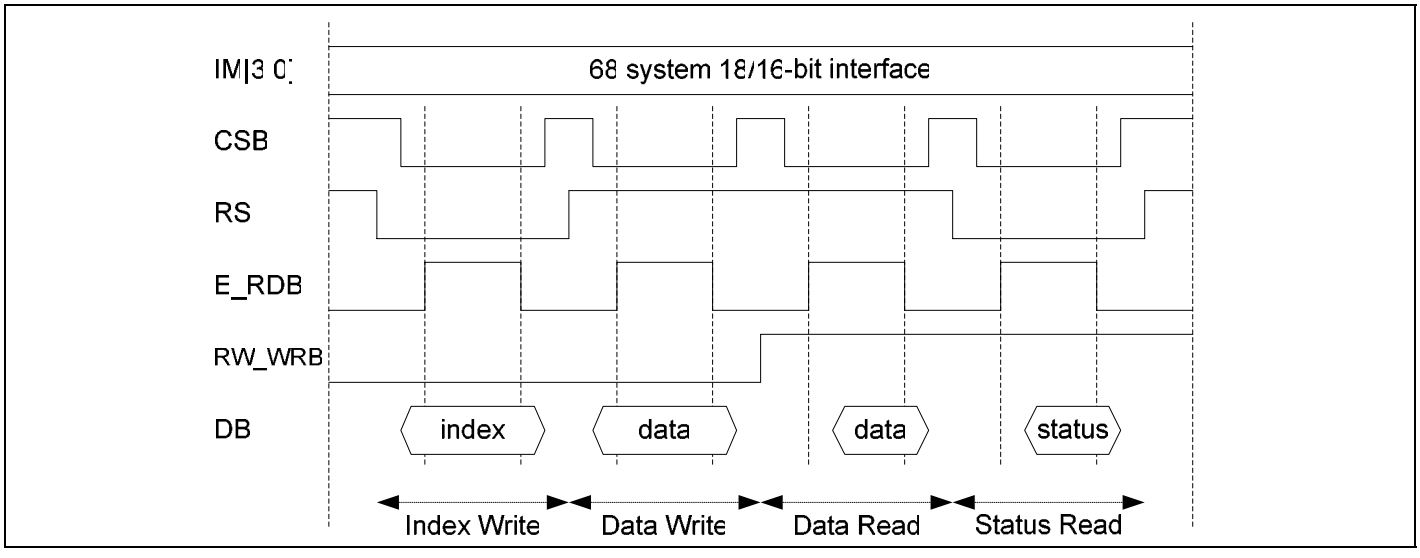


Figure 5.2.2.2.1 6800-Series Interface Data Bus Status (data read and write)

5.2.2.3 ACESS TO DISPLAY DATA RAM AND INTERNAL REGISTERS

Below figures show read/write accesses to the display data RAM and write accesses to internal registers 8-bit, 9-bit, 16-bit and 18-bit parallel interface modes.

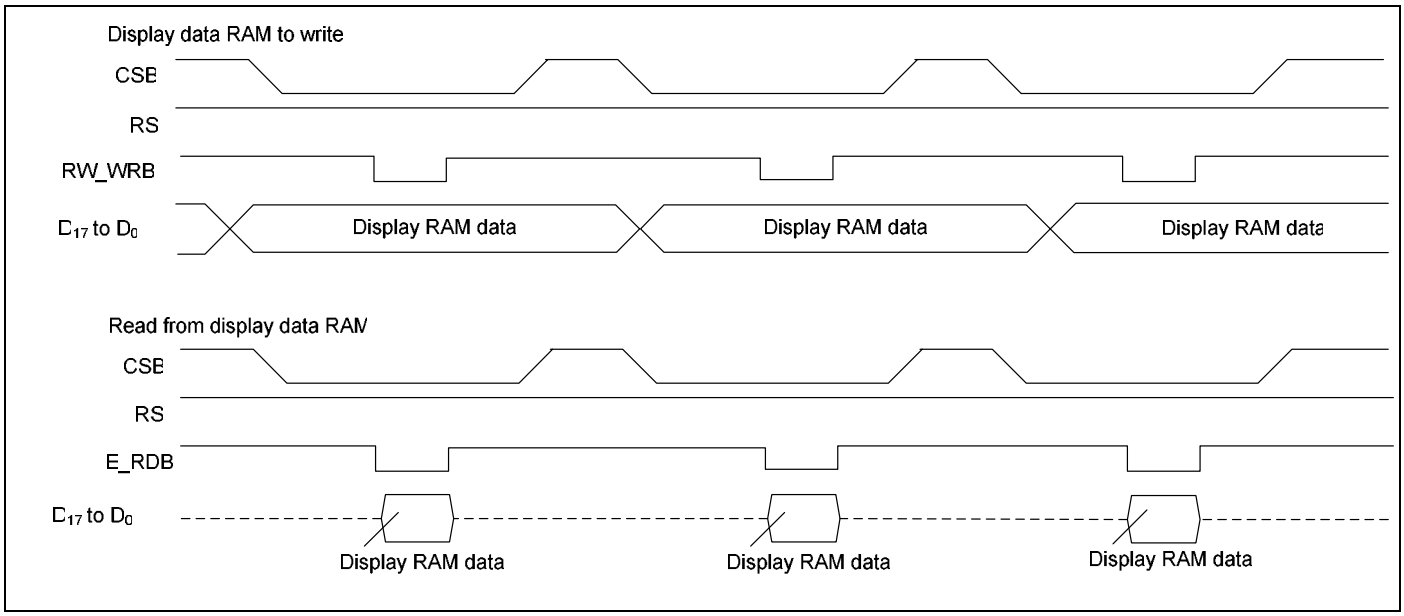


Figure 5.2.2.3.1 Read/Write in 16-/18-Bit parallel Interface (80-Series)

NOTE: While setting the writing to a display RAM, set it the fixed input of the high level to RS pin. While setting the writing to a display data RAM, in the case of 16-/18-bit parallel interface, 1 cycle period of write cycle is pointed out.

5.2.3 SERIAL INTERFACE

The S6D1121 allows serial interface transfer, using the chip select line (CSB), serial transfer clock line (SCL), register select line (RS), serial input data (SDI), and serial output data (SDO). For a serial interface, the IM0/ID pin function uses an ID pin.

The S6D1121 initiates serial data transfer by transferring the start byte at the falling edge of CSB input. It ends serial data transfer at the rising edge of CSB input. The S6D1121 is selected when the 6-bit chip address in the start byte matches the 6-bit device identification code that is assigned to the S6D1121. When selected, the S6D1121 receives the subsequent data string. The ID pin can determine the LSB of the identification code. The five upper bits must be 01110.

Two different chip addresses must be assigned to a single S6D1121 because the seventh bit of the start byte is used as a address select bit (DA): When DA = 0, data can be written to the index register or status can be read, and when DA = 1, an instruction can be issued or data can be written to or read from RAM. Read or write is selected according to the eighth bit of the start byte (RW_WRB bit). The data is received when the RW_WRB bit is 0, and is transmitted when the R/W bit is 1.

After receiving the start byte, the S6D1121 receives or transmits the subsequent data byte-by-byte. The data is transferred with the MSB first. The data after start byte consists of 16 bits (D15-0). Two bytes are received with the MSB first and the instructions are internally executed. After the start byte has been received, the next bytes are fetched of which, the first byte is fetched as the upper eight bits of D15-0 and the second byte is fetched as the lower eight bits of D15-0. Assignment into D15-0 is described in *Figure 5.2.3.1.3*.

Three bytes of RAM read data after the start byte are invalid. The S6D1121 starts to read correct RAM data from the fourth byte.

Table 5.2.3.1 Start Byte Format

Transfer Bit	1st	2nd	3rd	4th	5th	6th	7th	8th
Start byte format	Device Identification code						RS	RW_WRB
	0	1	1	1	0	ID		

NOTE: The IM [0] pin is used as ID

Table 5.2.3.2 RS bit and RW_WRB bit Function

RS bit	RW_WRB bit	Function
0	0	Set index register
0	1	Read status
1	0	Writes instruction or RAM data
1	1	Reads instruction or RAM data

5.2.3.1 SERIAL INTERFACE DATA FORMAT

Serial data is processed by 16-bit interface.

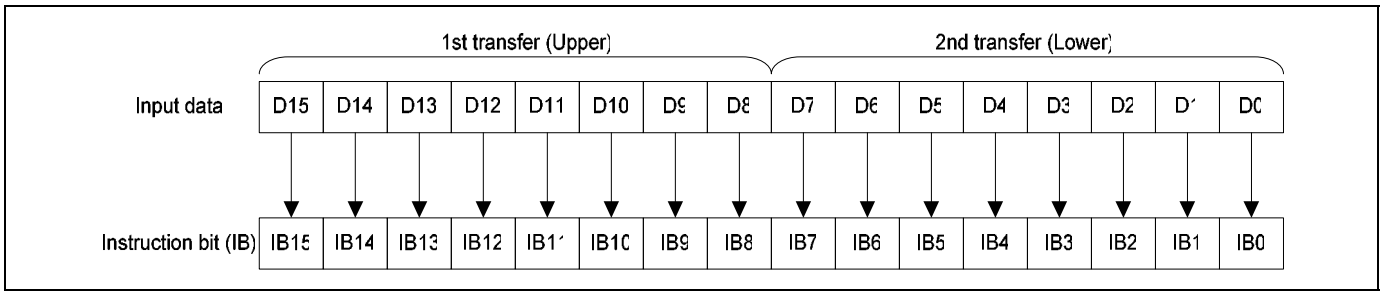


Figure 5.2.3.1.1 Instruction format for Serial Data Transfer

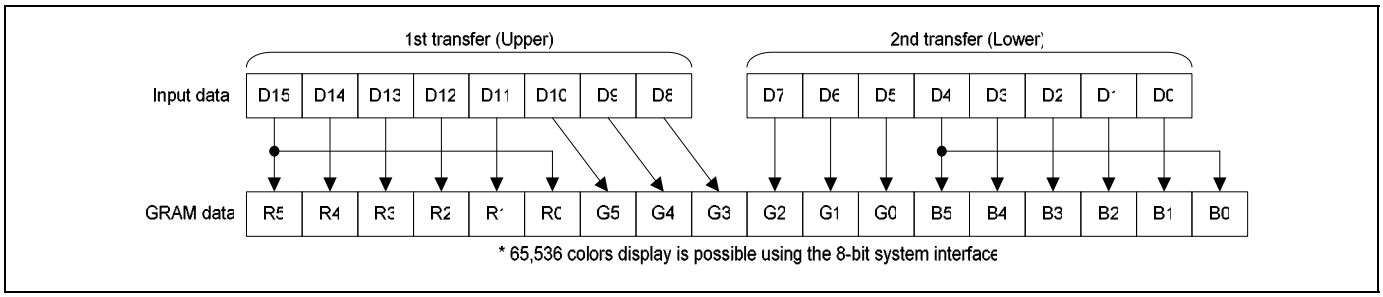


Figure 5.2.3.1.2 RAM Data Write format for Serial Data Transfer

Serial Interface Timing Diagram

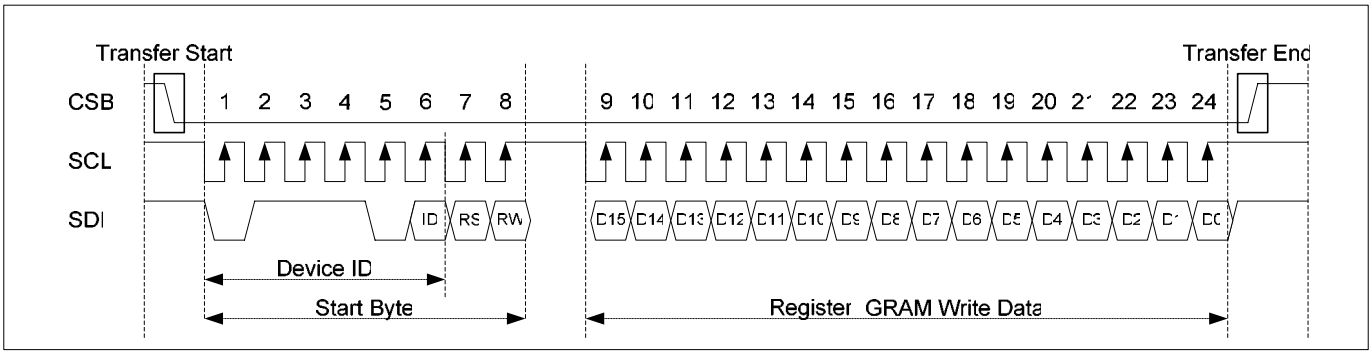


Figure 5.2.3.1.3 Basic Timing Diagram of Data Transfer through Serial Interface

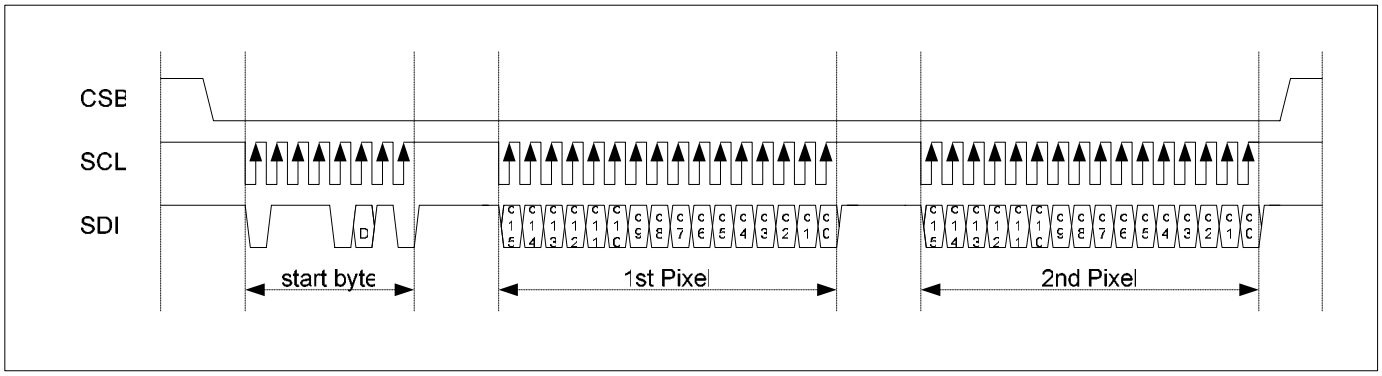


Figure 5.2.3.1.4 Timing Diagram of Consecutive RAM Data-Write through Serial Interface

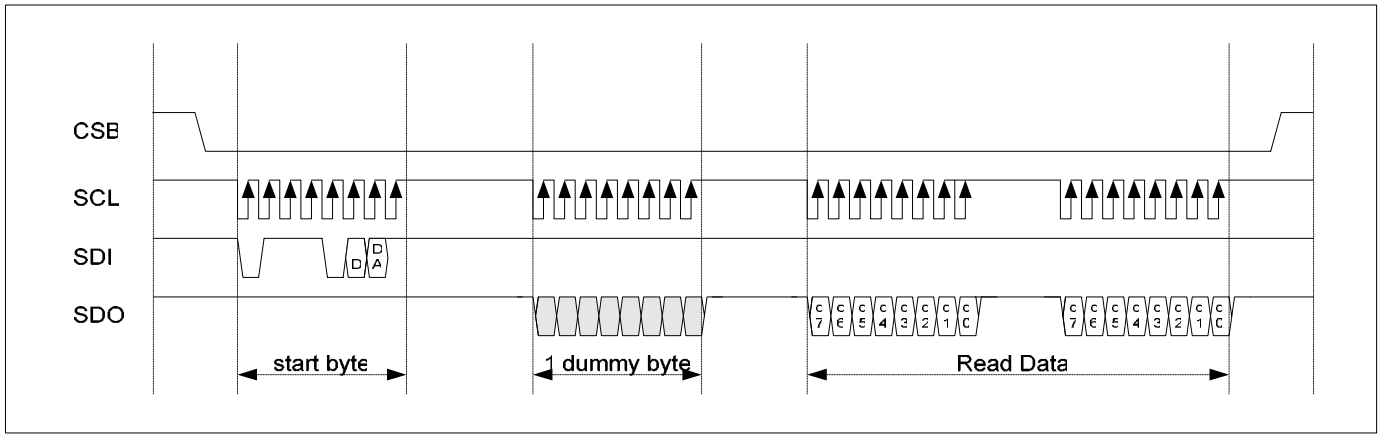


Figure 5.2.3.1.5 Timing Diagram of Register / Status Read through Serial Interface

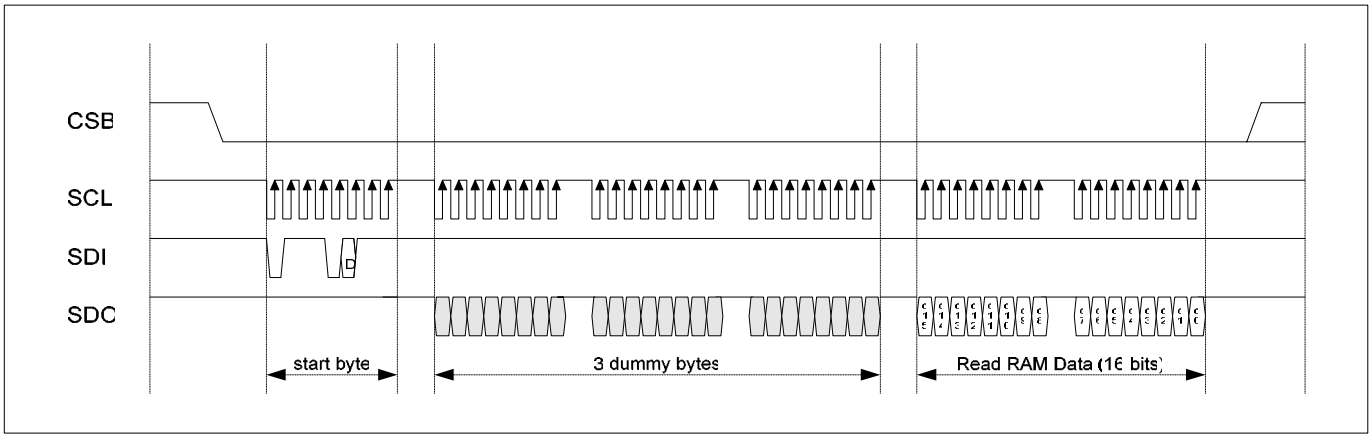


Figure 5.2.3.1.5 Timing Diagram of RAM-Data Read through Serial Interface

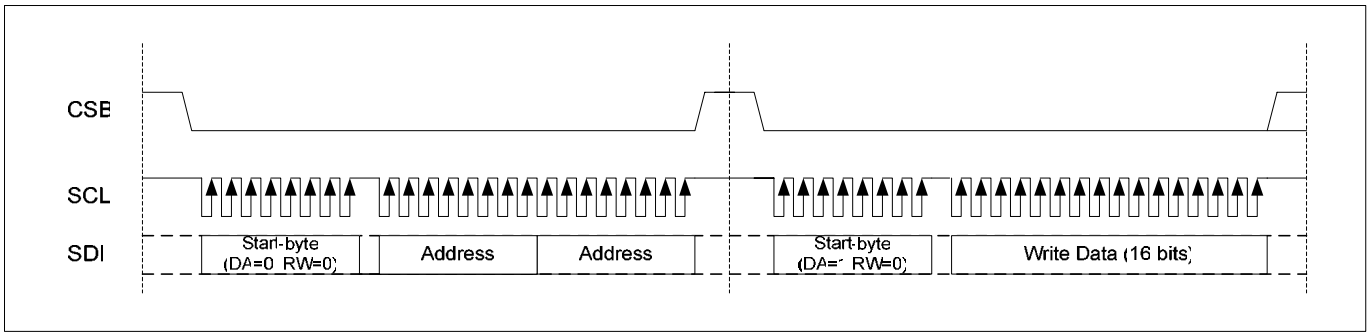


Figure 5.2.3.1.7 Timing Diagram of Register Write through Serial Interface

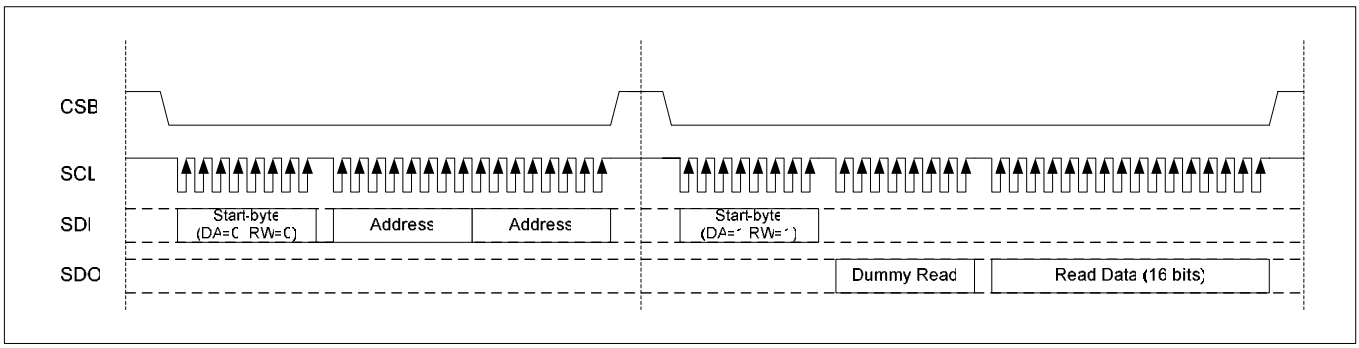


Figure 5.2.3.1.8 Timing Diagram of Register Read through Serial Interface

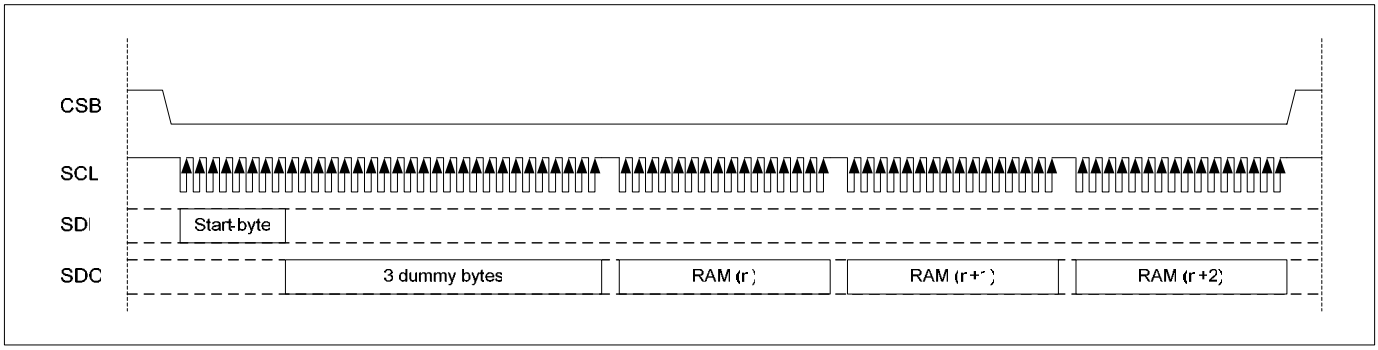


Figure 5.2.3.1.9 Timing Diagram of Consecutive RAM Data-Read through Serial Interface

5.2.4 RGB INTERFACE

S6D1121 incorporates RGB interface to display not only still pictures but also motion pictures and GRAM to store data for display. The RGB interface is performed in synchronization with VSYNC, HSYNC, and DOTCLK. Combining the function of the high-speed write mode and the window address enables transfer only the screen to be updated and reduce the power consumption.

Table 5.2.4.1 RIM Bits

RIM1	RIM0	RGB Interface	PD Pin
0	0	18-bit RGB interface	PD17 to 0
0	1	16-bit RGB interface	PD17 to13, 11 to 1
1	0	6-bit RGB interface	PD17 to12
1	1	Setting disabled	-

The relationship between EPL and ENABLE signal is shown below. When ENABLE is not active, the address is not update. When ENABLE is active, the address is updated.

Table 5.2.4.1 Relationship between EPL and ENABLE

EPL	ENABLE	RAM WRITE	RAM ADDRESS
0	0	Valid	Updated
0	1	Invalid	Hold
1	0	Invalid	Hold
1	1	Valid	Update

The below figure shows the RGB interface timing with ENABL signal. Window Address Function enables transfer only the screen to be updated and reduce the power consumption. This function must be setting the window address for window display area.

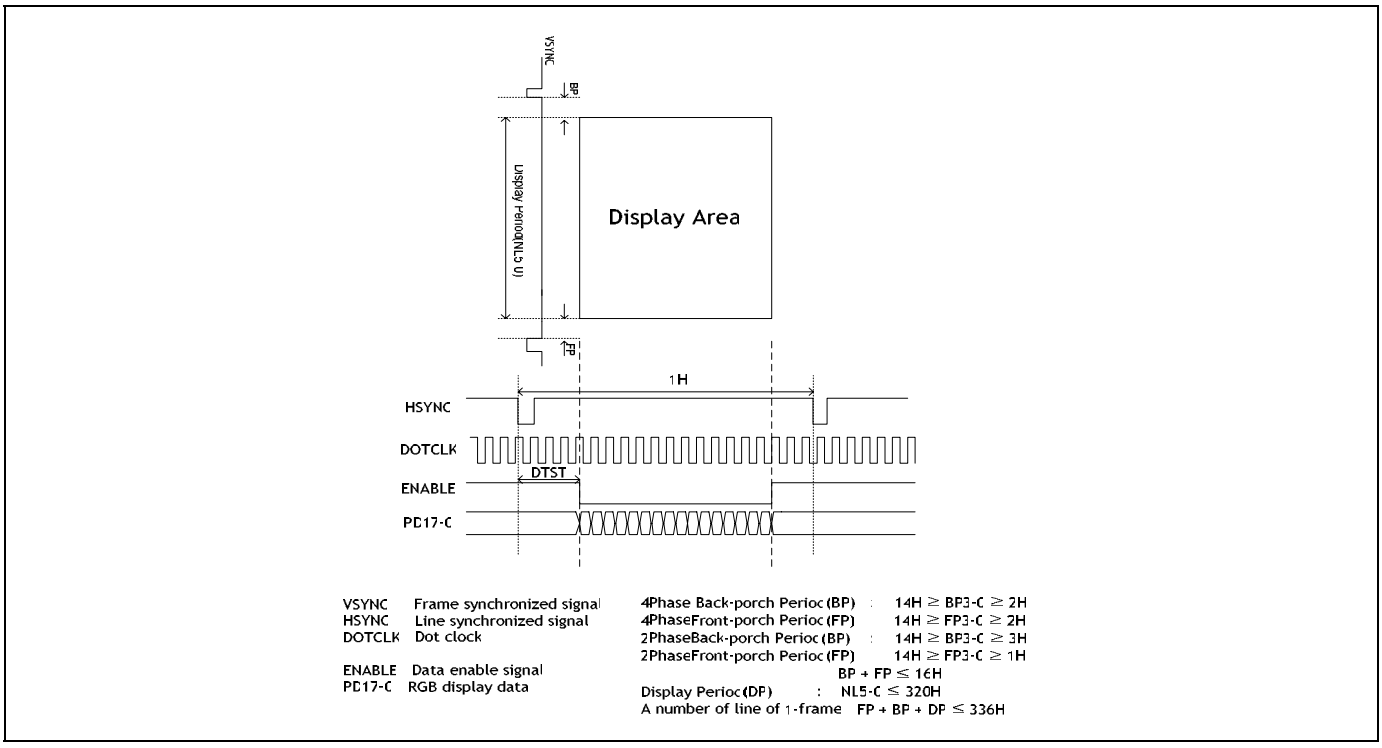


Figure 5.2.4.1 RGB Interface

NOTE: For RGB interface, VSYNC, HSYNC, DOTCLK should be supplied at much higher resolution than that of panel.

5.2.4.1 RGB INTERFACE TIMING

Time chart for RGB interface is shown below. (In case of EPL = 0)

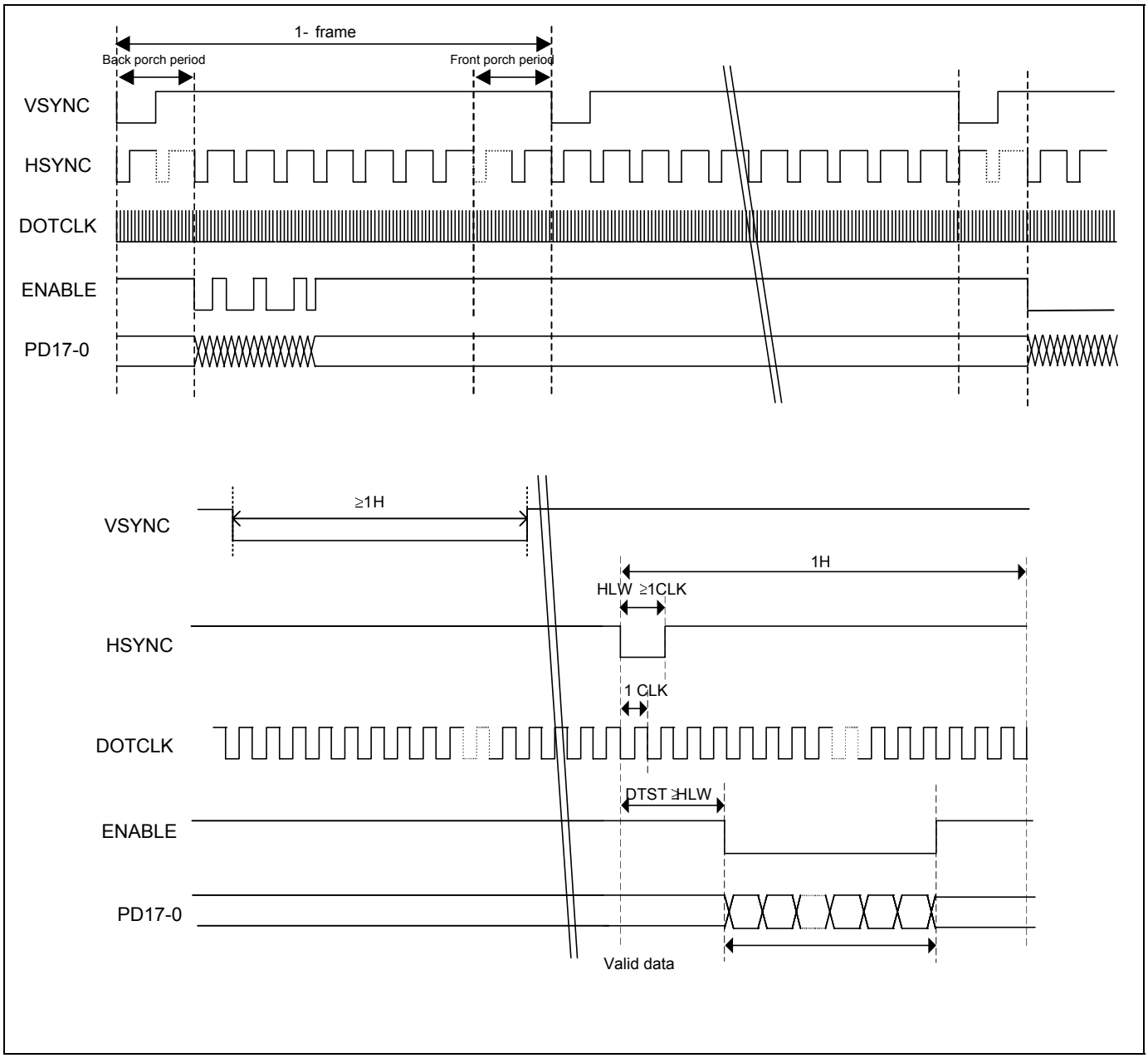


Figure 5.2.4.1.1 16-/18-bit RGB Interface Timing (In case of EPL = 0, DPL = 0, VSPL = 0, HSPL = 0)

VLW: The period in which VSYNC is “Low” level
HLW: The period in which HSYNC is “Low” level
DTST: Set up time of data transfer

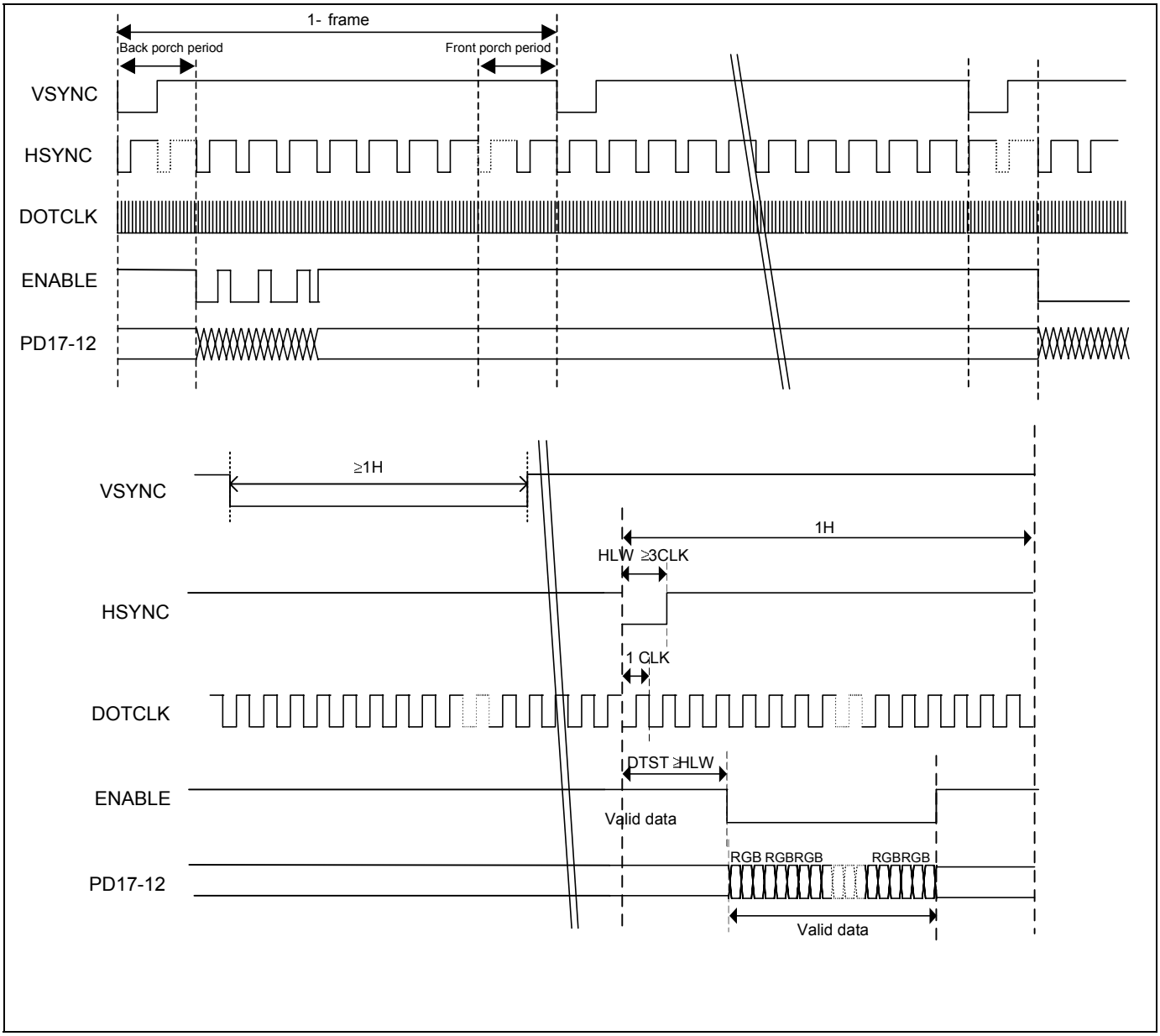


Figure 5.2.4.1.2 6-bit RGB Interface Timing (In case of EPL = 0, DPL = 0, VSPL = 0, HSPL = 0)

VLW: The period in which VSYNC is “Low” level
HLW: The period in which HSYNC is “Low” level
DTST: Set up time of data transfer

NOTES: 1. Three clocks are regarded as one clock for transfer when data is transferred in 6-bit interface.
2. VSYNC, HSYNC, ENABLE, DOTCLK and PD17-12 should be transferred in units of three clocks.

5.2.4.2 TRANSFER SYNCHRONIZATION

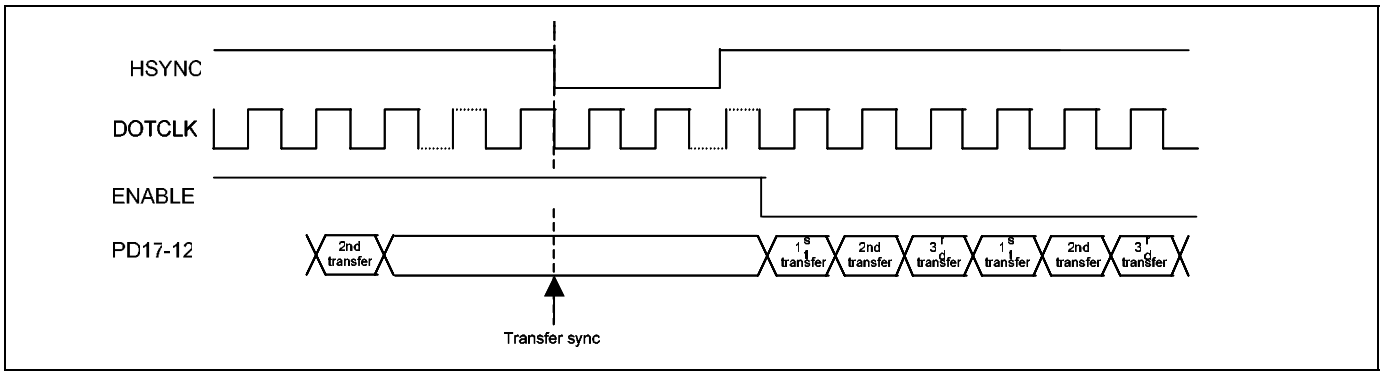


Figure 5.2.4.2.1 Transfer Synchronization Function in 6-bit RGB Interface Mode

NOTES:
1. Transfer synchronization function for a 6-bit bus interface. The S6D1121 has the transfer counter to count 1st, 2nd and 3rd data transfer in the 6-bit bus interface. The transfer counter is reset on the falling edge of VSYNC and enters the 1st data transmission state. Transfer mismatch can be corrected, and after that the transfer restarts correctly. In this method, when data such as displaying motion pictures is consecutively transferred, the effect of transfer mismatch is reduced and normal operation is recovered.
2. The internal display is operated in units of three DOTCLK. When the DOTCLK is not input in units of pixels, clock mismatch occurs and the frame, which is operated, and the next frame is not displayed correctly.

5.2.4.3 USAGE ON RGB DISPLAY INTERFACE

When external display interface is in use, the following functions are not available.

Table 5.2.4.3.1 External Display Interface and Internal Display Operation

Function	External (RGB) Display Interface	Internal Display Operation
Partial Display	Cannot be used	Can be used
Scroll Function	Cannot be used	Can be used
2 Interlace Driving	Cannot be used	Can be used

1. VSYNC, HSYNC, and DOTCLK signals should be supplied during display operation via RGB interface.

2. Please make sure that when setting bits ECS3-0 in RGB interface, the clock on which operations are based changes from the internal operating clock to DOTCLK.

3. RGB data are transferred for three clock cycles in 6-bit RGB interface. Data transferred, therefore, should be transferred in units of RGB.

4. Interface signals, VSYNC, HSYNC, DOTCLK, ENABLE and PD17-0 should be set in units of RGB (pixels) to match RGB transfer.

5. During the period between the completion of displaying one frame data and the next VSYNC signal, the display will remain for a front porch period.

An address set is done on the falling edge of VSYNC every frame in RGB interface.

5.2.5 VSYNC INTERFACE

The S6D1121 incorporates VSYNC interface, which enables motion pictures to be displayed with only the conventional system interface and the frame synchronization signal (VSYNC). This interface requires minimal changes from the conventional system to display motion pictures.

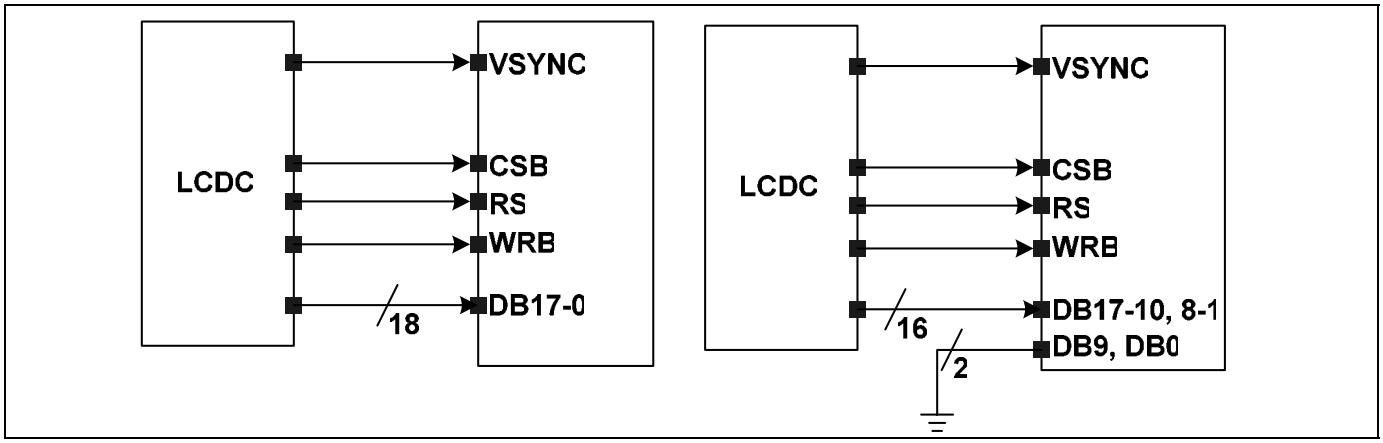


Figure 5.2.5.1 VSYNC Interface 18bit / 16bit (80 Systems)

When DM1-0=”10” and RM=”0”, VSYNC interface is available. In this interface the internal display operation is synchronized with VSYNC. Data for display is written to RAM via the system interface with higher speed than for internal display operation. This method enables flicker-free display of motion pictures with the conventional interface.

Display operation can be achieved by using the internal clock generated by the internal oscillator and the VSYNC input. Since, all the data for display is written to RAM, only the data to be rewritten is transferred. This method reduces the amount of data transferred during motion picture display operation.

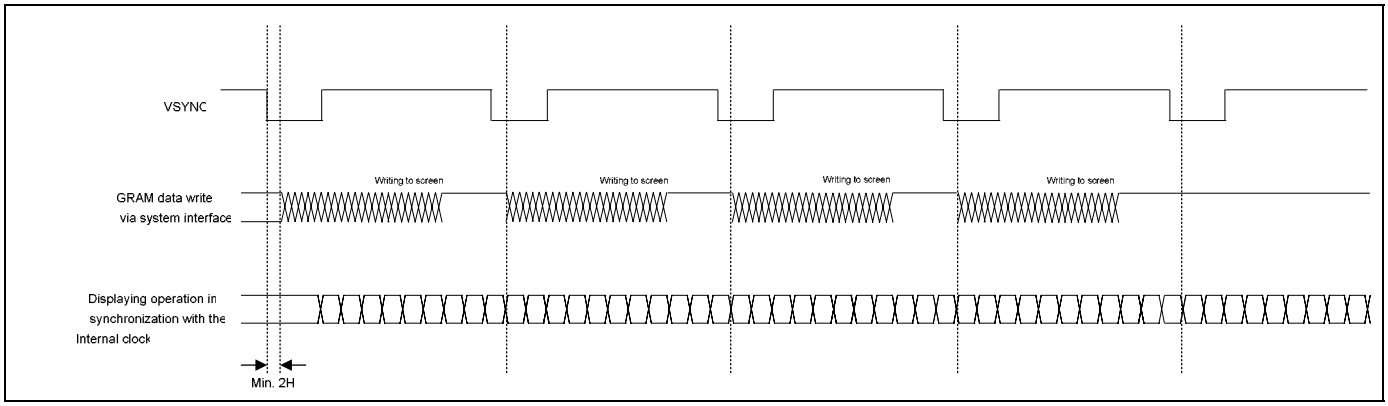


Figure 5.2.5.2 Motion Picture Data Transfer via VSYNC Interface

VSYNC interface requires taking the minimum speed for RAM writing via the system interface and the frequency of the internal clock into consideration. RAM writing should be performed with higher speed than the result obtained from the calculation shown below. The internal memory writing address counter is reset by VSYNC. So, ensure interval time between VSYNC falling and GRAM data writing. The minimum interval time is 2 raster rows, and hence the data writing should start only after that duration.

Internal clock frequency (fosc) [Hz] = Frame freq. × (Display raster-row (NL) + Front porch (FP) + Back porch (BP))
× 43-Clock × Fluctuation

Minimum speed for RAM writing [Hz] > 240 × Display raster-row (NL)
/ {((Back porch (BP) + Display raster-row (NL) – Margin) × 43 Clock) / fosc}

NOTE:

When RAM writing does not start immediately after the falling edge of VSYNC, the time between the falling edge of VSYNC and the RAM writing start timing must also be considered.

An example is shown below.

Example:

Display size	240RGB × 320 raster-rows
Display line number	320 raster-row (NL=100111)
Back/Front porch	4 lines/4 lines (BP=0100/FP=0100)
Frame Frequency	70Hz

Internal clock frequency (fosc) [Hz] = 70 Hz × (320 + 4 + 4) lines× 43 clock × 1.1 / 0.9 = 1.2 MHz

NOTES:

1.Calculating the internal clock frequency requires considering the fluctuation. In the above case a 10% fluctuation within the VSYNC period is assumed.
2.The fluctuation includes LSI production variation and air temperature fluctuation. Other fluctuations, including those for the external resistors and the supplied power, are not included in this example. Please keep in mind that a margin for these factors is also needed.

Minimum speed for RAM writing [Hz] > 240 × 320 / {((8 + 320 – 2) lines × 43 clock) / 1.2MHz} = 6.57 MHz

NOTES:

1. In this case RAM writing starts immediately after the falling edge of VSYNC.
2. The margin for display raster-row should be two raster-rows or more at the completion of RAM writing for one frame.

Therefore, when RAM writing starts immediately after the falling edge of VSYNC is performed at 6.57 MHz or more, the data for display can be rewritten before display operation has started. This means that flicker-free display operation is achieved.

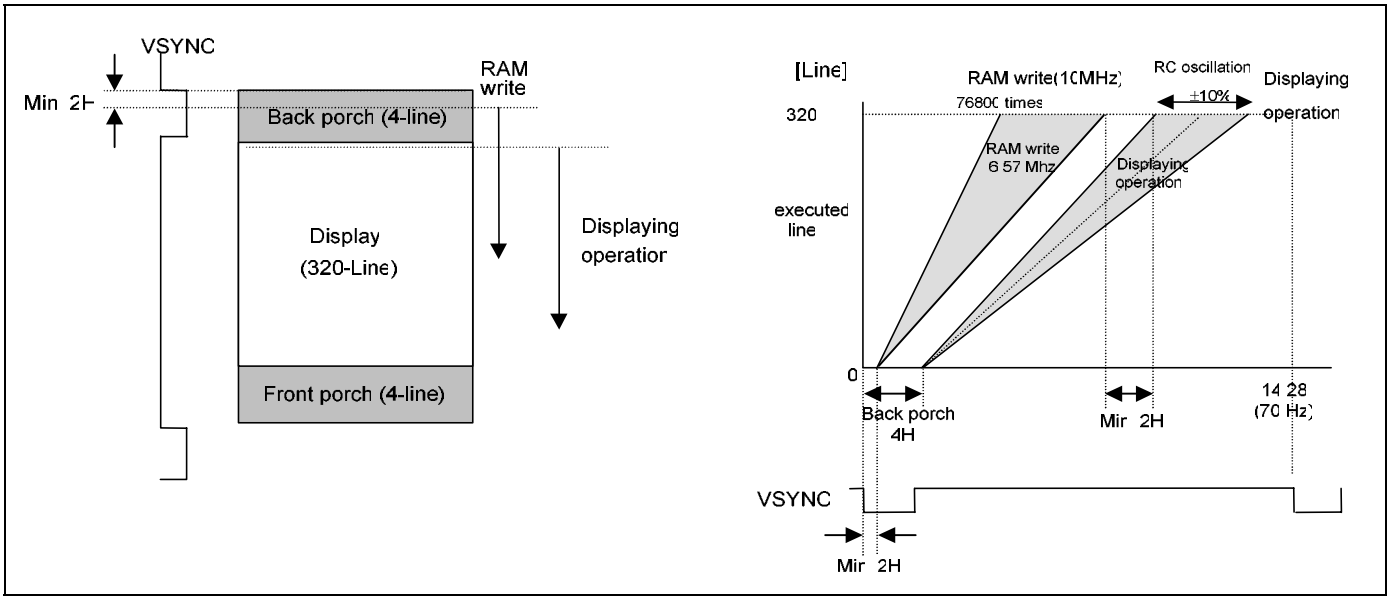


Figure 5.2.5.3 Operation for VSYNC Interface

5.2.5.1 USAGE ON VSYNC INTERFACE

When external display interface is in use, the following functions are not available.

Table 5.2.5.1.1 External Display Interface and Internal Display Operation

Function	External (VSYN IF) Display Interface	Internal Display Operation
Partial Display	Cannot be used	Can be used
Scroll Function	Cannot be used	Can be used
2 Interlace Driving	Cannot be used	Can be used

1. The example above is a calculated value. Please keep in mind that a margin for these factors is also needed. The reason of production variation of the internal oscillator requires consideration.

2. The example above is a calculated value of rewriting the whole screen. A limitation of the motion picture area generates a margin for the RAM write speed.

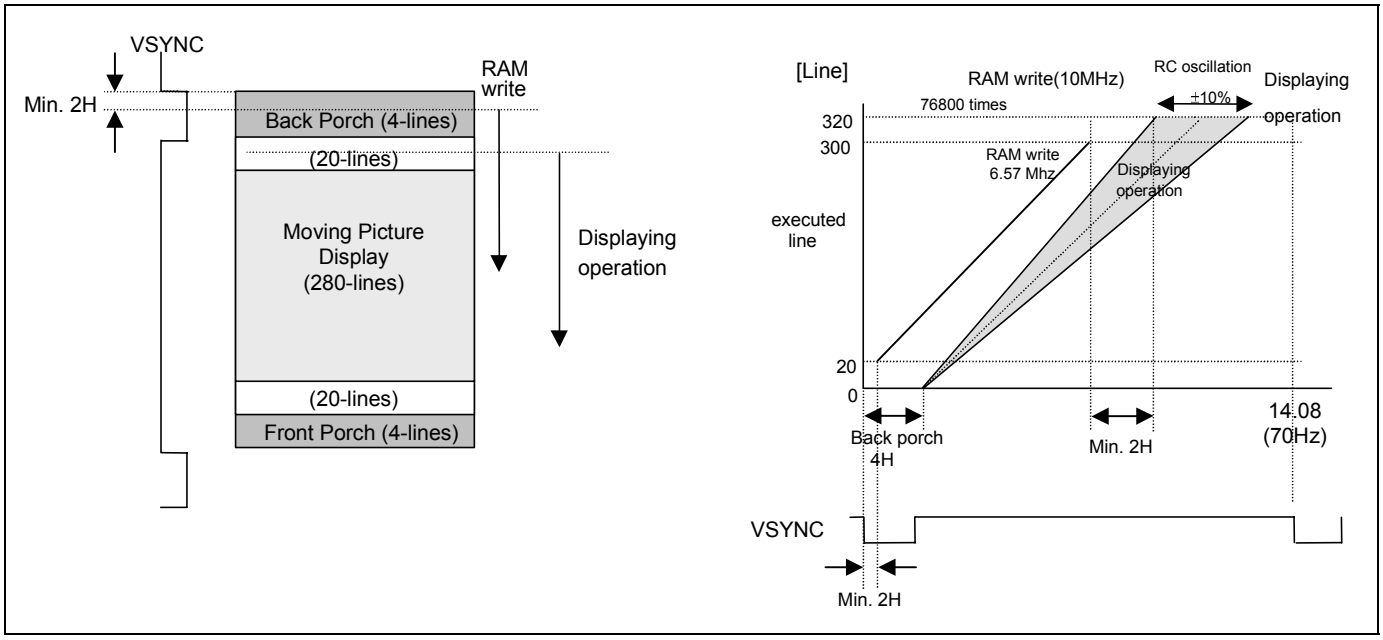


Figure 5.2.5.1.1 Limitation of Motion Picture Area

3. During the period between the completion of displaying one frame data and the next VSYNC signal, the display will remain for a front porch period.

4. Transition between the internal operating clock mode (DM1-0=”00”) and VSYNC interface mode will be valid after the completion of the screen, which is displayed when the instruction is set.

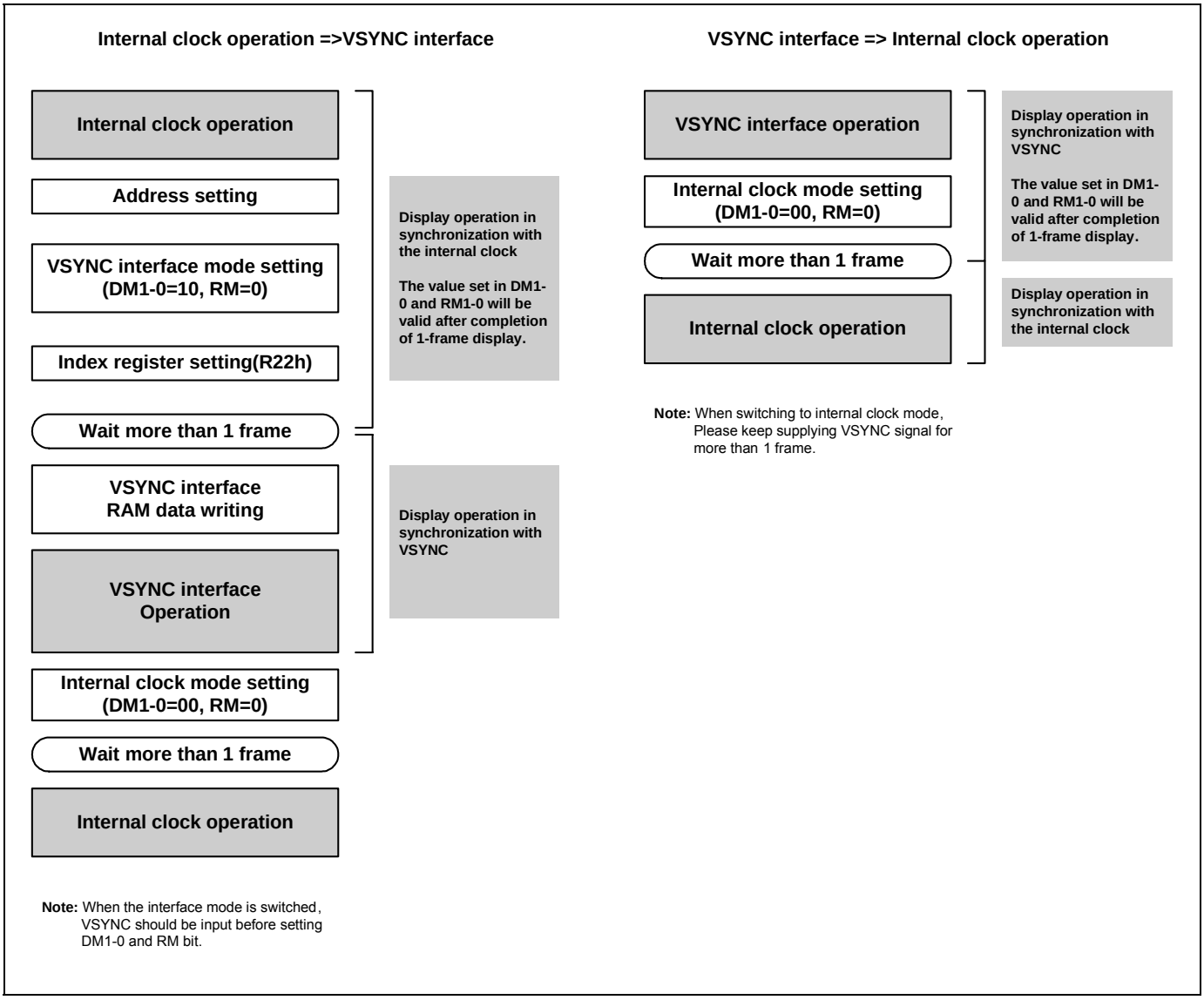


Figure 5.2.5.1.2 Transition between the Internal Operating Clock Mode and VSYNC Interface Mode

5. Partial display, vertical scroll, and interlaced driving functions are not available on VSYNC interface mode.

6. The flow of above method performs the VSYNC interface mode.

5.2.6 MDDI (MOBILE DISPLAY DIGITAL INTERFACE)

5.2.6.1 INTRODIUCTION OF MDDI

The S6D1121 supports MDDI. The MDDI is a differential and serial interface with high speed. Both command and image data transfer can be achieved with MDDI. MDDI host and client are linked with Data and STB line. Through data line, command or image data is transferred from MDDI host to MDDI client, and vice versa. Data is transferred by packet unit.
Through STB line, strobe signal is transferred. When the link is in “FORWARD direction”, data is transferred from host to client; in “REVERSE direction”, client transfer reverse data to MDDI host.

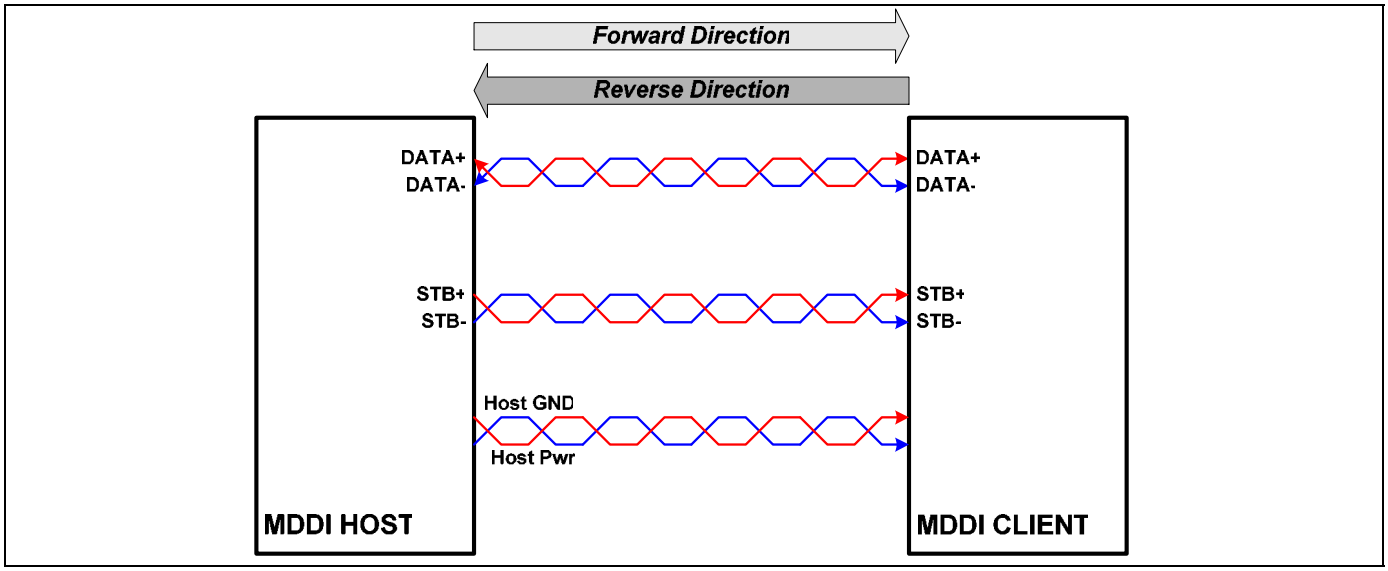


Figure 5.2.6.1.1 Physical connection of MDDI host and client

5.2.6.2 DATA-STB ENCODING

Data is encoded using a DATA-STB method. DATA is carried over a bi-directional differential cable, while STB is carried over a unidirectional differential cable driven only by the host. Figure below illustrates how the data sequence “1110001011” is transmitted using DATA-STB encoding.

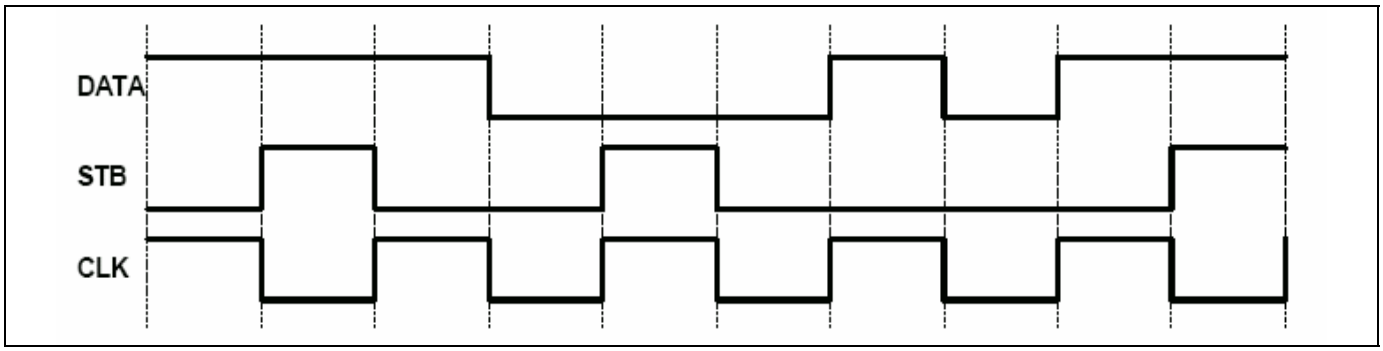


Figure 5.2.6.2.1 Data-STB encoding

The Following figure shows a sample circuit to generate DATA and STB from input data, and then recover the input data from DATA and STB.

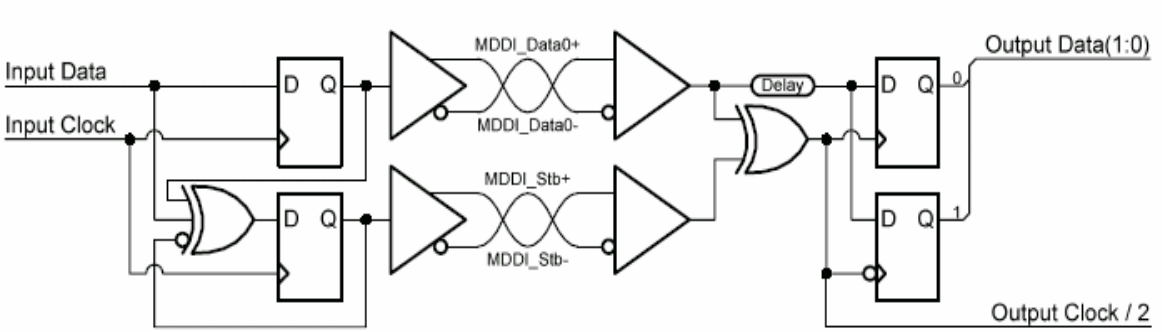


Figure 5.2.6.2.2 Data / STB Generation and Recovery circuit

5.2.6.3 MDDI DATA-STB

The Data (MDP/MDN) and STB (MSP/MSN) signals are always operated in a differential mode to maximize noise immunity. Each differential pair is parallel-terminated with the characteristic impedance of the cable. All parallel-terminations are in the client device. Figure below illustrates the configuration of the drivers, receivers, and terminations. The driver of each signal pair has a differential current output. While receiving MDDI packets the MDDI_DATA and MDDI_STB pairs use a conventional differential receiver with a differential voltage threshold of zero volts. In the hibernation state the driver outputs are disabled and the parallel termination resistors pull the differential voltage on each signal pair to zero volts. During hibernation a special receiver on the MDDI_DATA pairs has an offset input differential voltage threshold of positive 125 mV, which causes the hibernation line receiver to interpret the un-driven signal pair as logic-zero level.

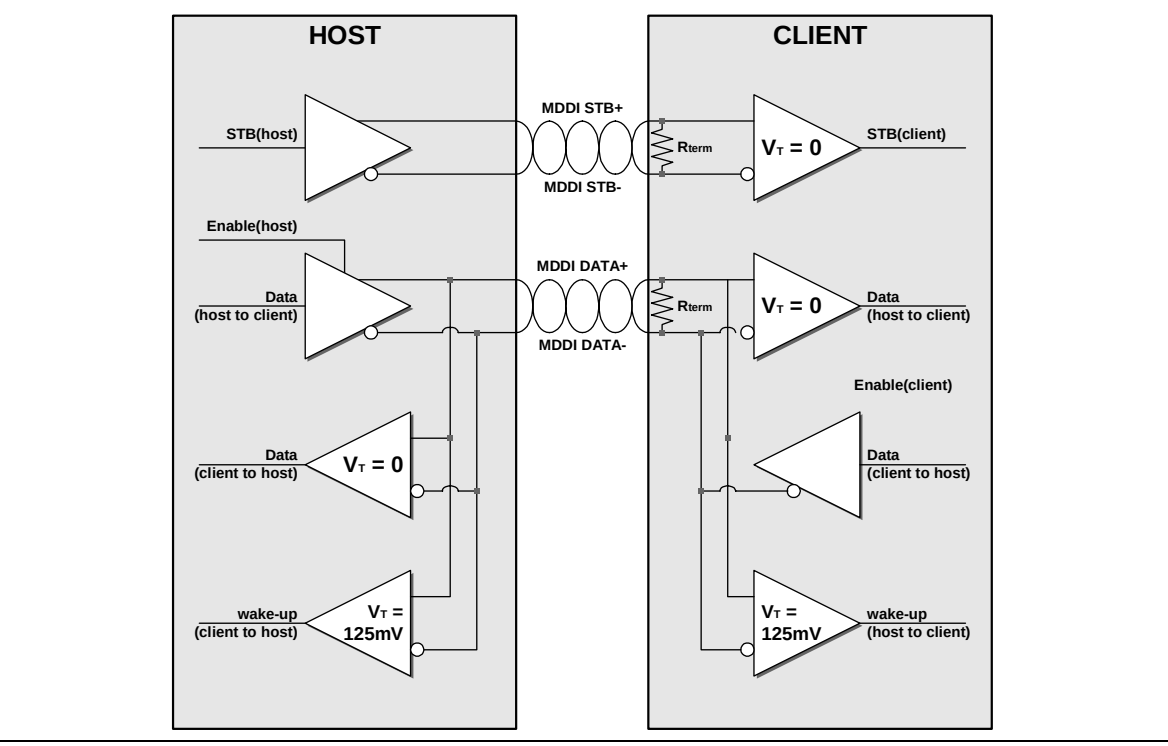


Figure 5.2.6.3.1 Differential connection between host and client

5.2.6.4 HIBERNATION AND WAKE_UP

S6D1121 support hibernation mode for reducing interface power consumption. The MDDI link can enter the hibernation state quickly and wake up from hibernation quickly. This allows the system to force the MDDI link into hibernation frequently to reduce power consumption.

In hibernation mode, hi-speed transceivers and receivers are disabled and low-speed & low-power receivers are enabled to detect wake-up sequence.

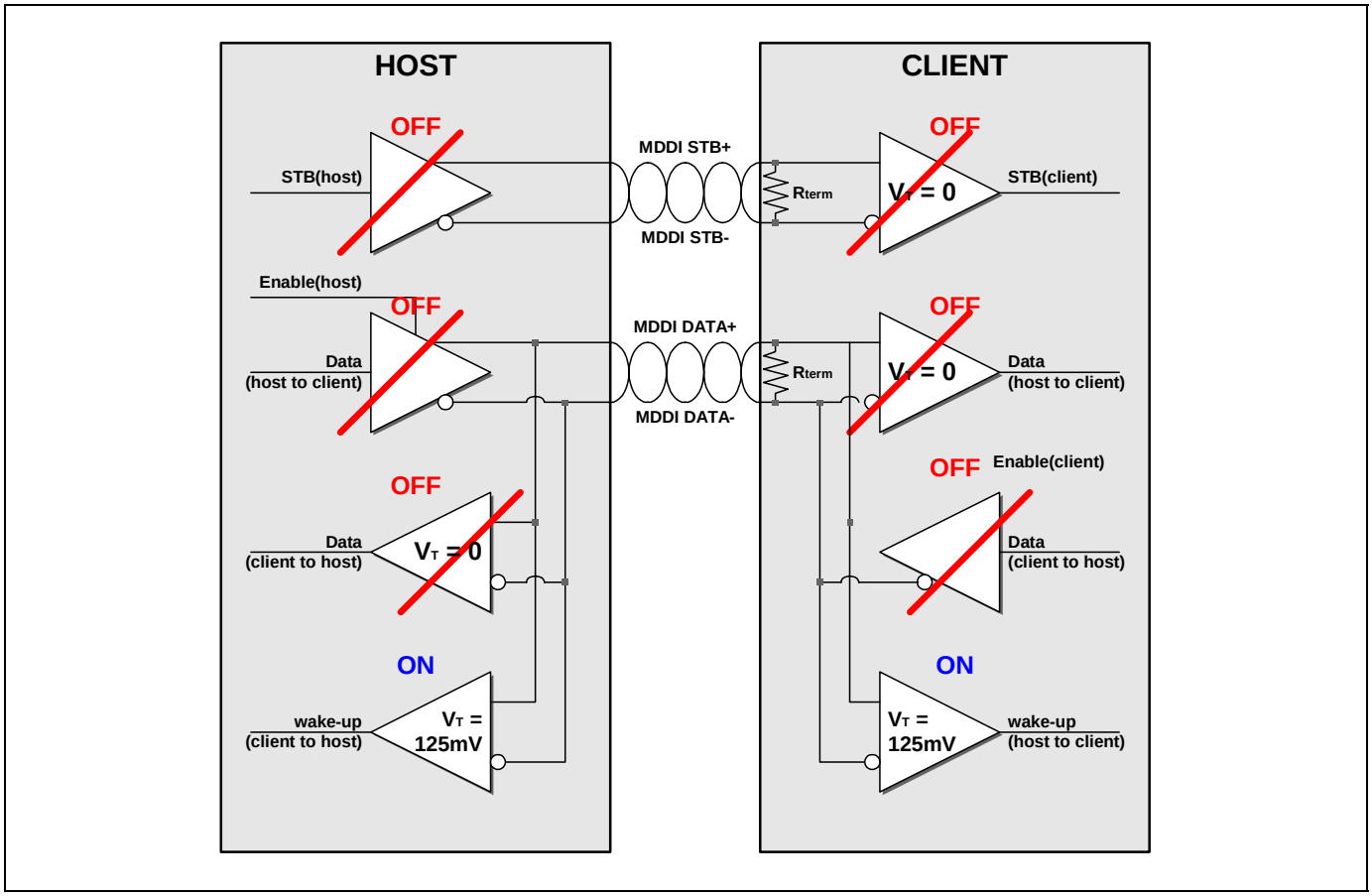


Figure 5.2.6.4.1 MDDI Transceiver and Receiver state in hibernation

When the link wakes up from hibernation the host and client exchange a sequence of pulses. These pulses can be detect using low-speed, low-power receivers that consume only a fraction of the current of the differential receivers required to receive the signals at the maximum link operating speed.

Both the client and the host can wake up the link, so 2-types of wake-up are supported in S6D1121: Host-initiated link wakeup and Client-initiated link wakeup.

5.2.6.5 MDDI LINK WAKE UP PROCEDURE

Rules for Entering the Hibernation State :

The host sends 64 MDDI_Stb cycles after the CRC of the Link Shutdown Packet. Also after this CRC the host shall drive MDDI_Data0 to a logic-zero level and disable the MDDI_Data0 output of the host in the range of after the rising edge of the 16th MDDI_Stb cycle to before the rising edge of the 48th MDDI_Stb cycle (including output disable propagation delays).

The host shall finish sending the 64 MDDI_Stb cycles after the CRC of the Link Shutdown packet before it initiates the wake-up sequence. The client shall wait until after the rigins edge of the 48th MDDI_Stb cycle after the CRC of the Link Shutdown Packet or later before it drives MDDI_Data0 to a logic-one level to attempt to wake-up the host.

The client shall place its high-speed receivers for MDDI_Data0 and MDDI_Stb into hibernation any time after the rising edge of the 48th MDDI_Stb cycle after the CRC of the Link Shutdown Packet. It is recommended that the client place its high-speed MDDI_Data0 and MDDI_Stb receivers into hibernation before the rising edge of the 64th MDDI_Stb cycle after the CRC of the Link Shutdown Packet.

Rules for Wake-up from the Hibernation State :

When the client needs service from the host it generates a request pulse by driving MDDI_Data0 to a logic-one level for 70 to 1000µsec while MDDI_Stb is inactive and keeps MDDI_Data0 driven to a logic-one level for 70 MDDI_Stb cycles(range of 60 to 80) after MDDI_Stb becomes active. Then the client disables the MDDI_Data0 driver by placing it into a high-impedance state.

If MDDI_Stb is active during hibernation(which is unlikely, but allowed per the spec) then the client may only drive MDDI_Data0 to a logic one level for 70 MDDI_Stb cycles (range of 60 to 80). This action causes the host to restart data traffic on the forward link and to poll the client for its status.

The host shall detect the presence of the request pulse from the client (using the low-power differential receiver with a +125mV offset) and begin the startup sequence by first driving MDDI_Stb to a logic-zero level and MDDI_Data0 to a logic-high level for at least 200nsec, and then while toggling MDDI_Stb it shall continue to drive MDDI_Data0 to a logic-one level for 150 MDDI_Stb cycles (range of 140 to 160) and to logic-zero for 50 MDDI_Stb cycles. The client shall not send a service request pulse if it detects MDDI_Data0 at a logic-one level for more than 80 MDDI_Stb cycles. After the client has detected MDDI_Data0 at a logic-one level for 60 to80 MDDI_Stb cycles it shall begin to search for the interval where drives MDDI_Data0 to a logic-zero level for 50 MDDI_Stb cycles then the host starts sending packets on the link. The first packet sent shall be a Sub-frame Header Packet. The client begins to look for the Sub-frame header Packet after MDDI_Data0 is at a logic-zero level for 40 MDDI_Stb cycles of the 50 cycle interval.

The host may initiate the wake-up by first enabling MDDI_Stb and simultaneously drive it to a logic-zero level. MDDI_Stb shall not be driven to a logic-one level until pulses are output as described below. After MDDI_Stb reaches a valid logic-zero level the host shall enable MDDI_Data0 and simultaneously drive it to a logic-one level. MDDI_Data0 shall not be driven to a logic-zero level during the wake-up process until the interval where it is driven to a logic-zero level for an interval of 50 MDDI_Stb pulses as described below. The host shall wait at least 200 nsec after MDDI_Data0 reaches a valid logic-one level before driving pulses on MDDI_Stb. This timing relationship shall always occur while considering the worst-case output enable delays. This guarantees that the client has sufficient time to fully enable its MDDI_Stb receiver after being woken up by a logic-one level on MDDI_Data0 that was driven by the host.

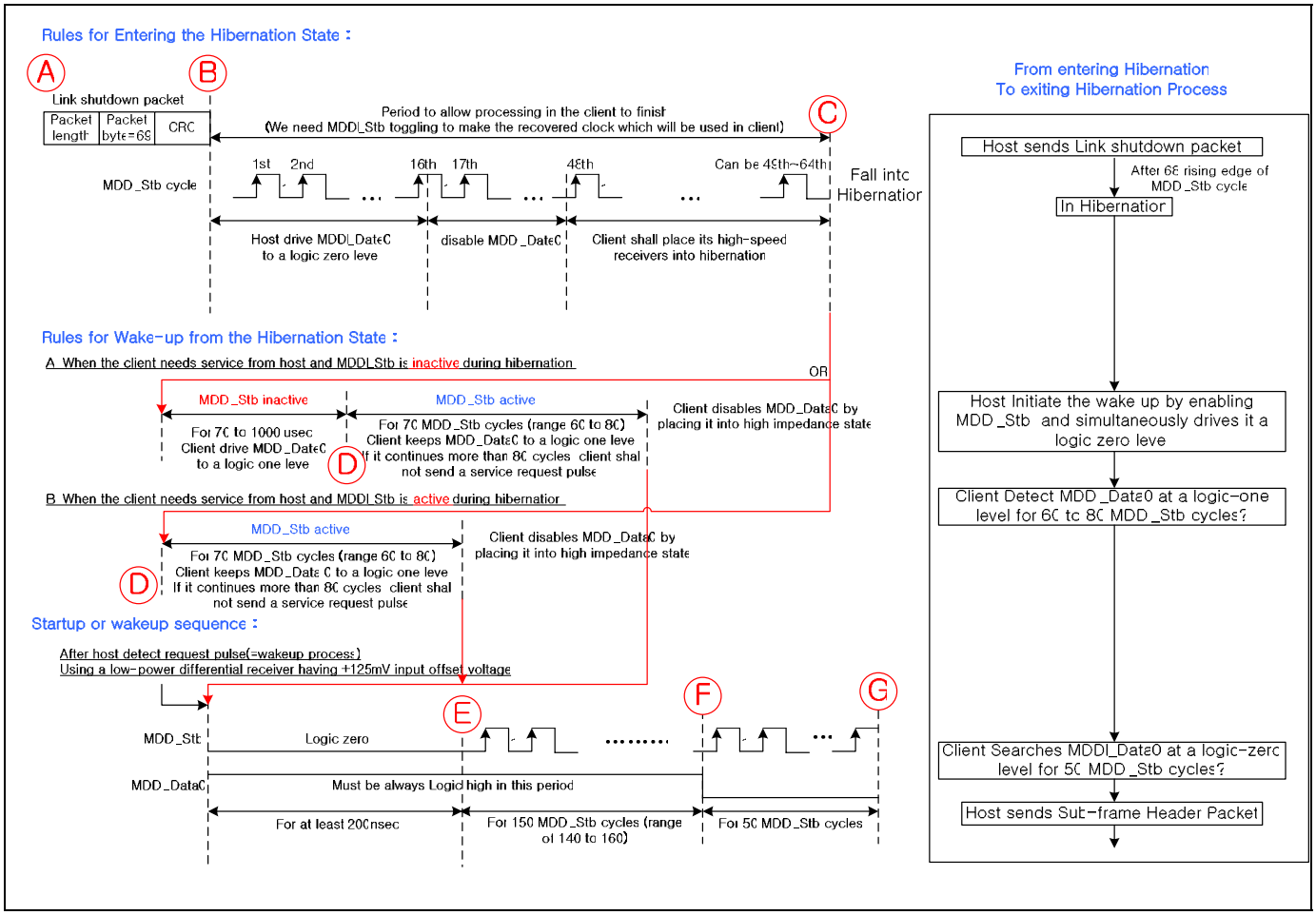


Figure 5.2.6.5.1 Process from Entering Hibernation to Exiting Hibernation

5.2.6.6 HOST-INITIATED LINK WAKE-UP PROCEDURE

The simple case of a host-initiated wake-up is described below without contention from the client trying to wake up at the same time. The following sequence of events is illustrated in the following figure.

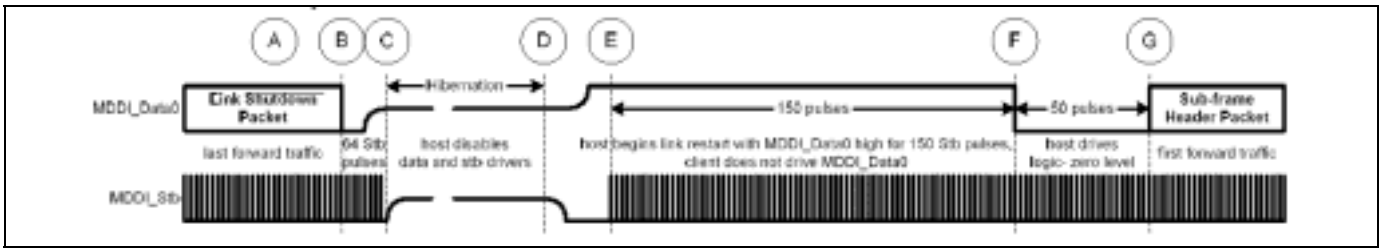


Figure 5.2.6.6.1 Host-initiated link wakeup sequence I

The detailed descriptions for labeled events are as follows:

A. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low-power hibernation state.

B. Following the CRC of the Link Shutdown Packet the host toggles MDDI_Stb for 64 cycles to allow processing in the client to finish before it stops MDDI_Stb from toggling which stops the recovered clock in the client device. Also during this interval the host initially sets MDDI_Data0 to a logic-zero level, and then disables the MDDI_Data0 output in the range of 16 to 48 MDDI_Stb cycles (including output disable propagation delays) after the CRC. It may be desirable for the client to place its high-speed receivers for MDDI_Data0 and MDDI_Stb into a low power state any time after 48 MDDI_Stb cycles after the CRC and before point C.

C. The host enters the low-power hibernation state by disabling the MDDI_Data0 and MDDI_Stb drivers and by placing the host controller into a low-power hibernation state. It is also allowable for MDDI_Stb to be driven to logic-zero level or to continue toggling during hibernation. The client is also in the low-power hibernation state.

D. After a while, the host begins the link restart sequence by enabling the MDDI_Data0 and MDDI_Stb driver outputs. The host drives MDDI_Data0 to a logic-one level and MDDI_Stb to logic-zero level for at least the time it takes for the drivers to fully enable their outputs. The host shall wait at least 200 nsec after MDDI_Data0 reaches a valid logic-one level and MDDI_Stb reaches a valid logic-zero level before driving pulses on MDDI_Stb. This gives the client sufficient time to prepare to receive high-speed pulses on MDDI_Stb. The client first detects the wake-up pulse using a low-power differential receiver having a +125mV input offset voltage.

E. The host drivers are fully enabled and MDDI_Data0 is being driven to a logic-one level. The host begins to toggle MDDI_Stb in a manner consistent with having a logic-zero level on MDDI_Data0 for a duration of 150 MDDI_Stb cycles.

F. The host drives MDDI_Data0 to logic-zero level for 50 MDDI_Stb cycles. The client begins to look for the Sub-frame Header Packet after MDDI_Data0 is at logic-zero level for 40 MDDI_Stb cycles.

G. The host begins to transmit data on the forward link by sending a Sub-frame Header Packet. Beginning at point G the MDDI host generates MDDI_Stb based on the logic level on MDDI_Data0 so that proper data-strobe encoding commences from point G.

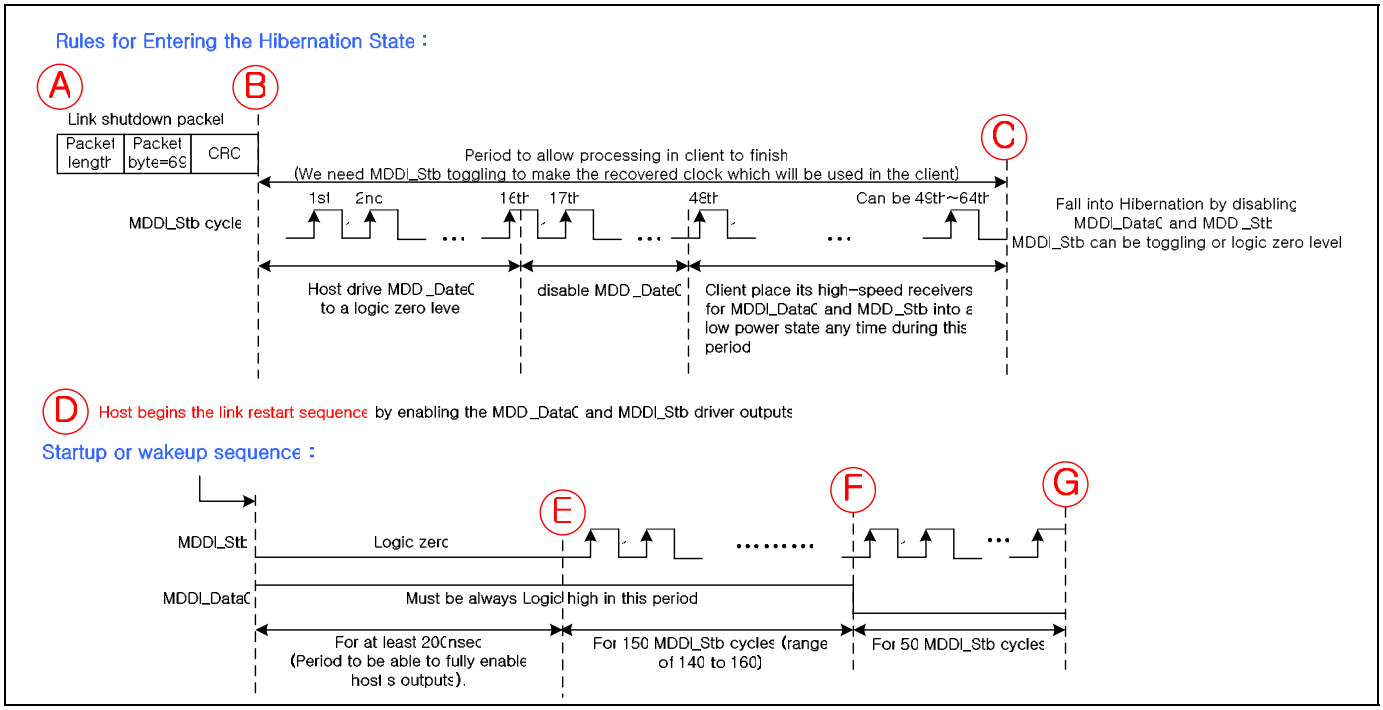


Figure 5.2.6.6.2 Host-initiated link wakeup sequence II

5.2.6.7 CLIENT INITIATED LINK WAKE-UP PROCEDURE

An example of a typical client-initiated service request event with no contention is illustrated in the following figure.

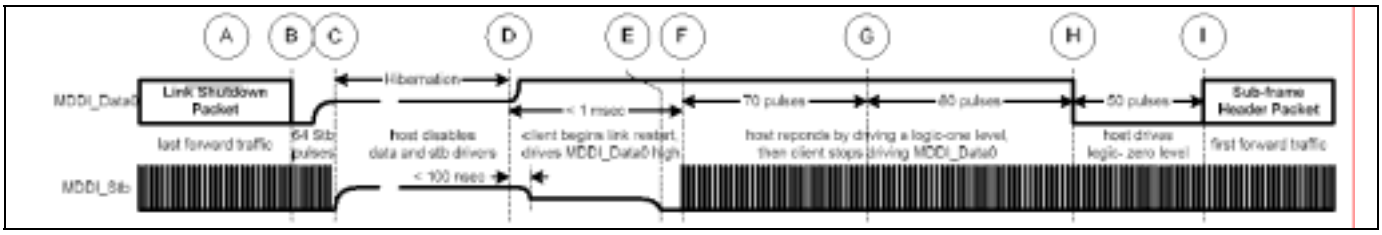


Figure 5.2.6.7.1 Client-initiated link wakeup sequence

The Detailed descriptions for labeled events are as follows:

A. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low-power hibernation state.

B. Following the CRC of the Link Shutdown Packet the host toggles MDDI_Stb for 64 cycles to allow processing in the client to finish before it stops MDDI_Stb from toggling which stops the recovered clock in the client device. Also during this interval the host initially sets MDDI_Data0 to a logic-zero level, and then disables the MDDI_Data0 output in the range of 16 to 48 MDDI_Stb cycles (including output disable propagation delays) after the CRC. It may be desirable for the client to place its high-speed receivers for MDDI_Data0 and MDDI_Stb into a low power state any time after 48 MDDI_Stb cycles after the CRC and before point C.

C. The host enters the low-power hibernation state by disabling its MDDI_Data0 and MDDI_Stb driver outputs. It is also allowable for MDDI_Stb to be driven to logic-zero level or to continue toggling during hibernation. The client is also in the low-power hibernation state.

D. After a while, the client begins the link restart sequence by enabling the MDDI_Stb receiver and also enabling an offset in its MDDI_Stb receiver to guarantee the state of the received version of MDDI_Stb is a logic-zero level in the client before the host enables its MDDI_Stb driver. The client will need to enable the offset in MDDI_Stb immediately before enabling its MDDI_Stb receiver to ensure that the MDDI_Stb receiver in the client is always receiving a valid differential signal and to prevent erroneous received signals from propagating into the client. After that, the client enables its MDDI_Data0 driver while driving MDDI_Data0 to a logic-one level. It is allowed for MDDI_Data0 and MDDI_Stb to be enabled simultaneously if the time to enable the offset and enable the standard MDDI_Stb differential receiver is less than 200 nsec.

E. Within 1 msec the host recognizes the service request pulse, and the host begins the link restart sequence by enabling the MDDI_Data0 and MDDI_Stb driver outputs. The host drives MDDI_Data0 to a logic-one level and MDDI_Stb to a logic-zero level for at least the time it takes for the drivers to fully enable their outputs. The host shall wait at least 200 nsec after MDDI_Data0 reaches a valid logic-one level and MDDI_Stb reaches a valid fully-driven logic-zero level before driving pulses on MDDI_Stb. This gives the client sufficient time to prepare to receive high-speed pulses on MDDI_Stb.

F. The host begins outputting pulses on MDDI_Stb and shall keep MDDI_Data0 at a logic-one level for a total duration of 150 MDDI_Stb pulses through point H. The host generates MDDI_Stb in a manner consistent with sending a logic-zero level on MDDI_Data0. When the client recognizes the first pulse on MDDI_Stb it shall disable the offset in its MDDI_Stb receiver.

G. The client continues to drive MDDI_Data0 to a logic-one level for 70 MDDI_Stb pulses, and the client disables its MDDI_Data0 driver at point G. The host continues to drive MDDI_Data0 to a logic-one level for duration of 80 additional MDDI_Stb pulses, and at point H drives MDDI_Data0 to logic-zero level.

H. The host drives MDDI_Data0 to logic-zero level for 50 MDDI_Stb cycles. The client begins to look for the Sub-frame Header Packet after MDDI_Data0 is at logic-zero level for 40 MDDI_Stb cycles. After asserting MDDI_Data0 to logic-zero level and driving MDDI_Stb for duration of 50 MDDI_Stb pulses the host begins to transmit data on the forward link at point I by sending a Sub-frame Header Packet. The client begins to look for the Sub-frame Header Packet after MDDI_Data0 is at logic-zero level for 40 MDDI_Stb cycles.

It will be possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then S6D1121 will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select Line is released after a whole byte of a command as been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below.

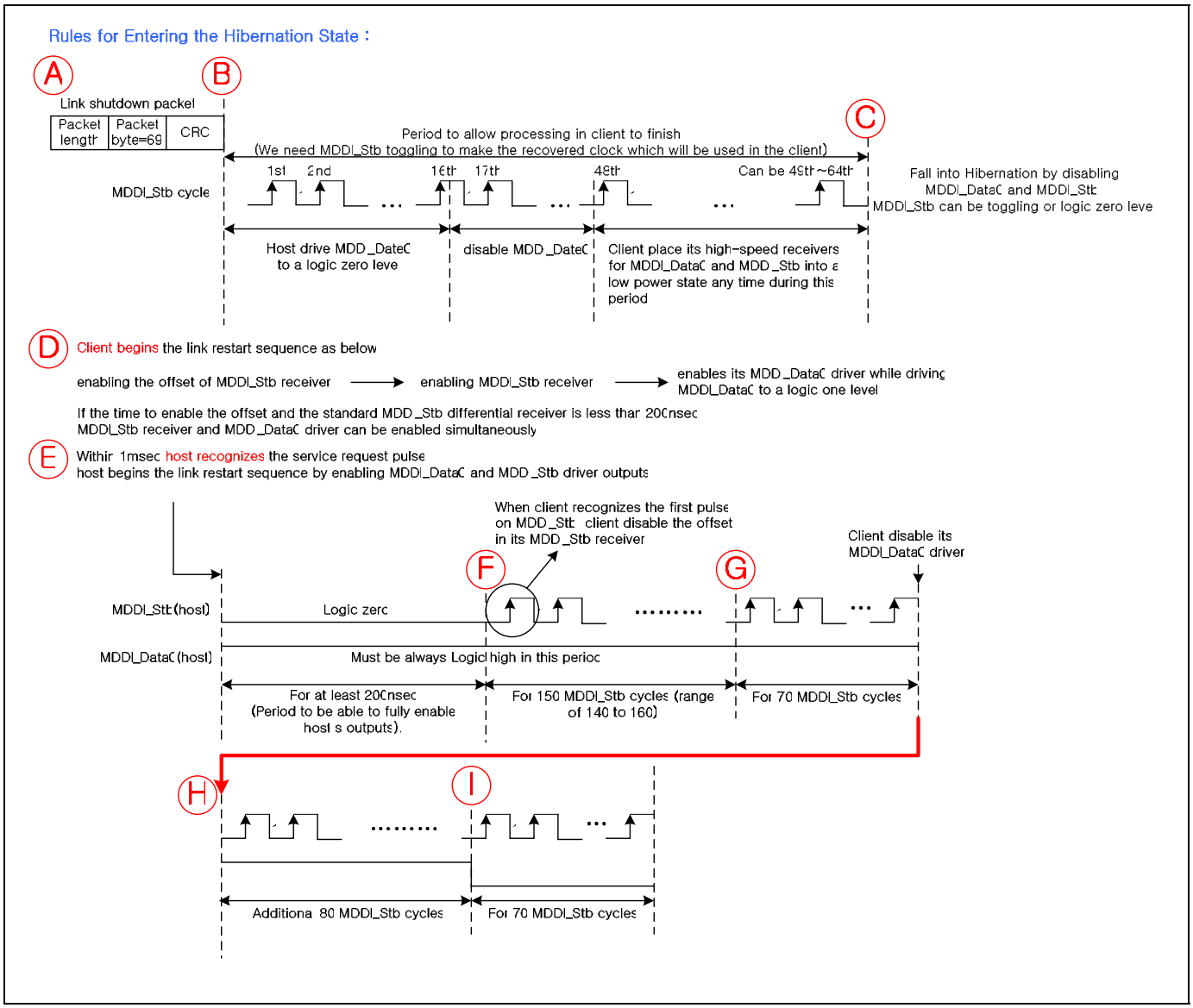


Figure 5.2.6.7.2 Client-initiated Wakeup Sequence

S6D1121 supports 1-type of client-initiated link wake-up: VSYNC based Link Wake-up. As client-initiated wake-up action is executed in hibernation state only, register setting for each wake-up have to be set before link shut-down.

Vsync Based Link Wake Up:

In display-ON state, when the IC finishes displaying all internal GRAM data, data request must be transferred to MDDI host for new video data. As MDDI link is usually in hibernation for reducing interface power consumption, MDDI link wake-up must be done before internal GRAM update. In that case, client initiated link wake-up can be used as data request.

When VSYNC based link wake-up register (50h: VWAKE_EN) is set, client initiated wake-up is executed in synchronization with the vertical-sync signal which generated in S6D1121. Using VSYNC based link wake-up, tearing-less display can be accomplished if interface speed and wake-up time is well known.

The following figure shows detailed timing for VSYNC based link wake-up.

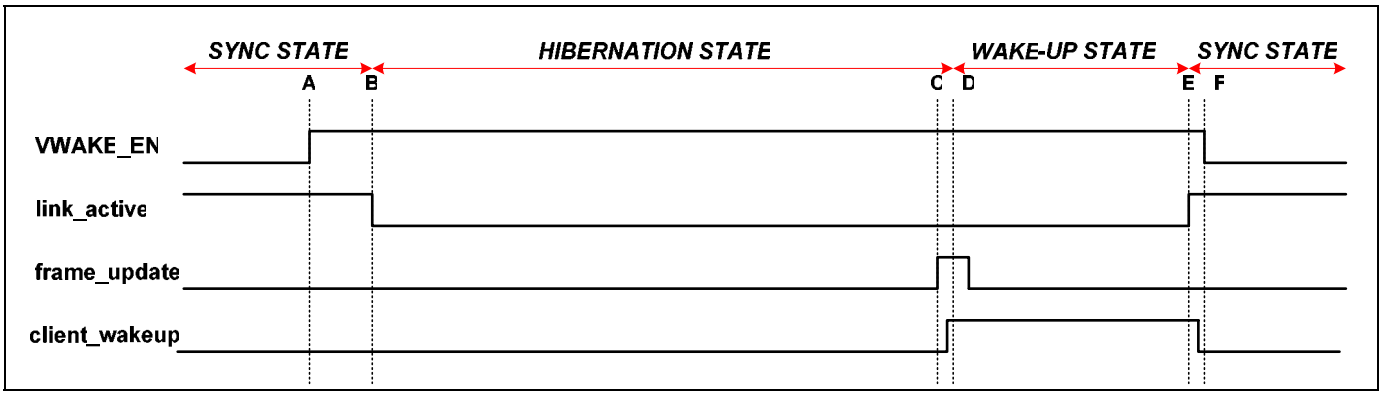


Figure 5.2.6.7.3 VSYNC based Link Wake-Up Procedure

The Detailed descriptions for labeled events are as follows:

A. MDDI host writes to the VSYNC based link wakeup register to enable a wake-up based on internal vertical-sync signal.

B. link_active goes low when the host puts in the link into hibernation after no more data needs to be sent to the S6D1121.

C. frame_update, the internal vertical-sync signal goes high indicating that update pointer has wrapped around and is now reading from the beginning of the frame buffer. Link wake-up point can be set using WKF and WKL (51h) registers. WKF specifies the number of frame before wake-up; WKL specifies the number of lines before wake-up.

D. client_wakeup input to the MDDI client goes high to start the client initiated link wake-up.

E. link_active goes high after the host brings the link out of hibernation.

F. After link wake-up, client_wakeup signal and the VWAKE_EN register are cleared automatically.
It will be possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then S6D1121 will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select Line is released after a whole byte of a command as been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below.

5.2.6.8 HOST-INITIATED WAKE-UP FROM HIBERNATION WITH CONNECTION FROM CLIENT

This is actually a host-initiated wake-up, but we have included the case where the client also wants to wake up the link with the latest possible request. The labeled events are:

A. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low-power hibernation state.

B. Following the CRC of the Link Shutdown Packet the host toggles MDDI_Stb for 64 cycles to allow processing in the client to finish before it stops MDDI_Stb from toggling which stops the recovered clock in the client device. Also during this interval the host disables the MDDI_Data0 output in the range of 16 to 48 MDDI_Stb cycles(including output disable propagation delays) after the CRC. It may be desirable for the client to place its high-speed receivers for MDDI_Data0 and MDDI_Stb into a low power state any time after 48 MDDI_Stb cycles after the CRC and before point C.

C. The host enters the low-power hibernation state by disabling its MDDI_Data0 and MDDI_Stb driver outputs. It is also allowable for MDDI_Stb to be driven to a logic-zero level or to continue toggling during hibernation. The client is also in the low-power hibernation state.

D. After a while, the host begins the link restart sequence by enabling the MDDI_Data0 and MDDI_Stb driver outputs. The host drives MDDI_Data0 to a logic-one level and MDDI_Stb to a logic-zero level for at least the time it takes for the drivers to fully enable their outputs. The host shall wait at least 200 nsec after MDDI_Data0 reaches a valid logic-one level and MDDI_Stb reaches a valid logic-zero level before driving pulses on MDDI_Stb. This gives the client sufficient time to prepare to receive high-speed pulses on MDDI_Stb.

E. The host drivers are fully enabled and MDDI_Data0 is being driven to a logic-one level. The host begins to toggle MDDI_Stb in a manner consistent with having a logic-zero level on MDDI_Data0 for a duration of 150 MDDI_Stb cycles.

F. At up to 70 MDDI_Stb cycles after point E the client has not yet recognized that the host is driving MDDI_Data0 to a logic-one level so the client also drives MDDI_Data0 to a logic-one level. This occurs because the client has a need to request service from the host and does not recognize that the host has already begun the link restart sequence.

G. The client ceases to drive MDDI_Data0, and places its driver into a high-impedance state by disabling its output. The host continues to drive MDDI_Data0 to a logic-one level for 80 additional MDDI_Stb cycles.

H. The host drives MDDI_Data0 to a logic-zero level for 50 MDDI_Stb cycles. The client begins to look for the Sub-frame Header Packet after MDDI_Data0 is at a logic-zero level for 40 MDDI_Stb cycles.

I. The host begins to transmit data on the forward link by sending a Sub-frame Header Packet. Beginning at point I the MDDI host generates MDDI_Stb based on the logic level on MDDI_Data0 so that proper data-strobe encoding commences from point I.

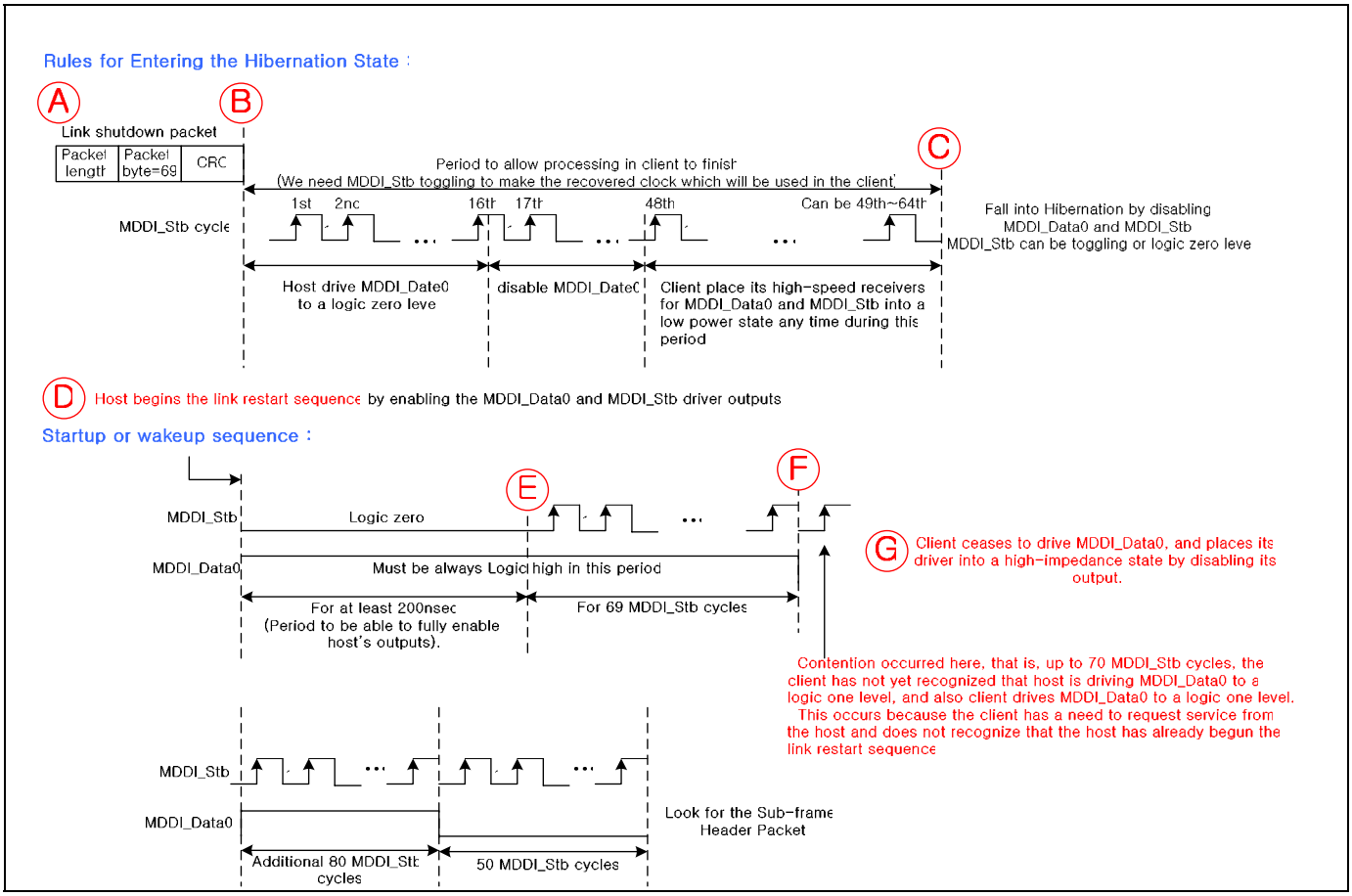


Figure 5.2.6.8.1 Host-Initiated Wake-up Process from Hibernation with Connection from Client

5.2.6.9 MDDI PACKET

MDDI transfer data by packet format. MDDI host can make many packets and transfer them. In S6D1121, several packets format is supported. Most packets are transferred from MDDI host to client (forward direction); but reverse encapsulation packet is transferred from MDDI client to host (reverse direction).

A number of packets, started by sub-frame header packet, construct 1 sub frame.

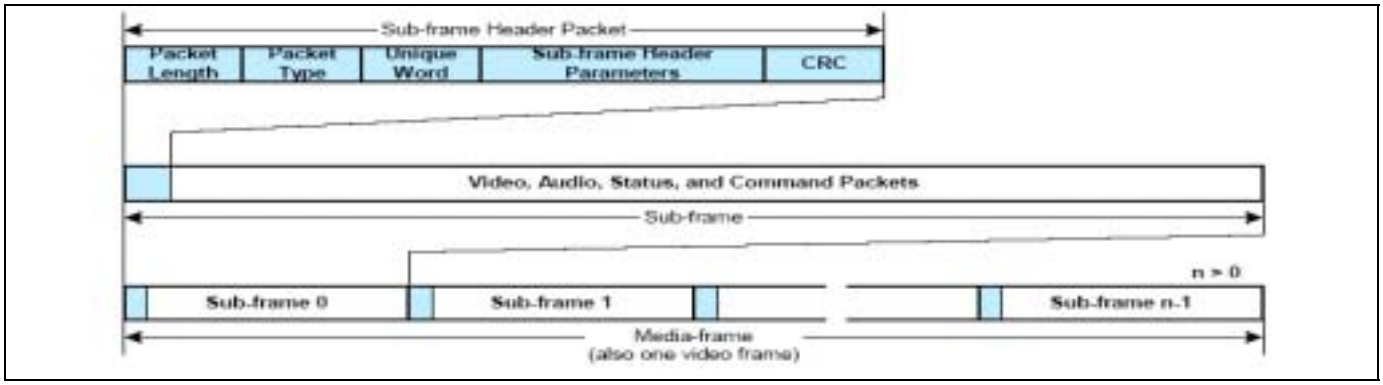


Figure 5.2.6.9.1 Host-Initiated Wake-up Process from Hibernation with Connection from Client

Refer to MDDI packet structure, sub-frame header packet is placed in front of a sub-frame, and some sub-frame construct media-frame together.
The following table describes 9 types of packet which is supported in S6D1121.

PACKET	FUNCTION	DIRECTION
Sub-frame header packet	Header of each sub frame	Forward
Register access packet	Register setting	Forward
Video stream packet	Video data transfer	Forward
Filler packet	Fill empty packet space	Forward
Reverse link encapsulation packet	Reverse data packet	Reverse
Round-trip delay measurement packet	Host->client->host delay check	Forward/Reverse
Client capability packet	Capability of client check	Reverse
Client request and status packet	Information about client status	Reverse
Link shutdown packet	End of frame	Forward

Sub-frame header packet:

packet length	packet type = 3bffh	unique word = 005ah	reserved1	sub-frame length	protocol version	sub-frame count	media frame count	CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	2 bytes	4 bytes	2 bytes

packet length : packet length not including packet length block
packet type : packet type (sub-frame header packet is 3bffh)
unique word : Identify "This packet is sub-frame header packet"
reserved1 : not used (set zero)
sub-frame length : specifies number of bytes per sub-frame
protocol version : set all zero
sub-frame count : specifies number of sub-frame header packet
mddi frame count : specifies number of media frames
CRC : error check

Figure 5.2.6.9.2 Sub-frame header packet structure

Register Access Packet:

packet lengtr	packet type = 146	bClient ID	Read/Write Infc	Register Address	Paramter CRC	Register Data List	Register Data CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	4 bytes	2 bytes

packet length : packet length not including packet length block
packet type : packet type(Register Access packet is 146(decimal))
bClient ID : set to all zerc
Read/Write Info : to write register value, bits[15:14] = "00'
to read register value, bits[15:14] = "11'
bits[13:0] is all zerc
Register Address : Register address is set written here.
Parameter CRC : To error check from packet length to register address
Register Data List : Paramter data is written here.
CRC : To error check register data list

Figure 5.2.6.9.3 Register access packet structure

Video Stream Packet:

packet length	packet type= 16	bClientID	video data formal descriptor	pixel data attributes	X left edge	Y top edge	X right edge	Y bottom edge	X start	Y start
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes

pixel count	parameter CRC	pixel data	pixel data CRC
2 bytes	2 bytes	packet length - 26 bytes	2 bytes

packet length packet length not including packatet length block
packet type packet type(video stream packet is 16)
bClientID reserved set all 0
video data format descriptor bits[15 13] = 010 raw RGB format(fixed value)
bits[12] = 1 Only packed type is available(fixed value)
bits[11 0] = 0110_0110_0110 18 bit pixel
bits[11 0] = 0101_0110_0101 16 bit pixel
pixel data attributes bits[1 0] = 11 displayed both eyes(fixed value)
bits[5] = 1 X left edge . Y start edge is not defined.(fixed value)
other bits are all zero
X left edge Not used in S6D1121 set all zero
Y top edge Not used in S6D1121 set all zero
X right edge Not used in S6D1121 set all zero
Y bottom edge Not used in S6D1121 set all zero
X start Not used in S6d1121 set all zero
Y start Not used in S6d1121 set all zero
Pixel count Write number of pixel
Paramter CRC To error check from packet length to pixel count
pixel data pixel data info number of pixel data must not be over 65509
pixel data CRC To pixel data error check

Figure 5.2.6.9.4 Video stream packet structure

Filler Packet:

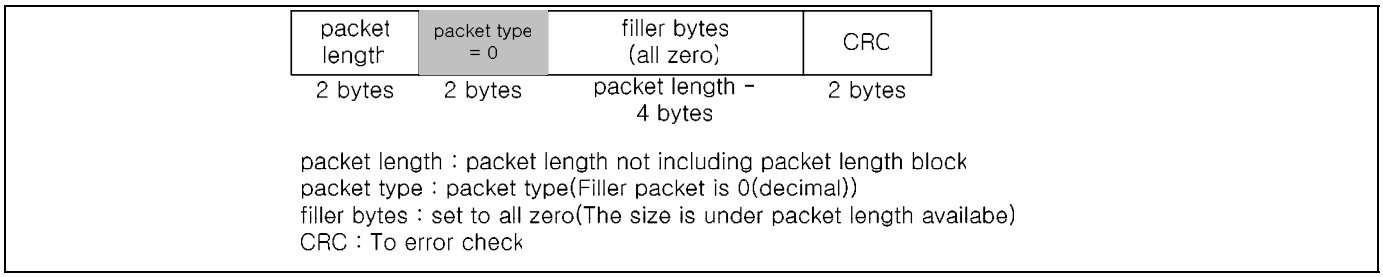


Figure 5.2.6.9.5 Filler packet structure

Link Shutdown Packet:

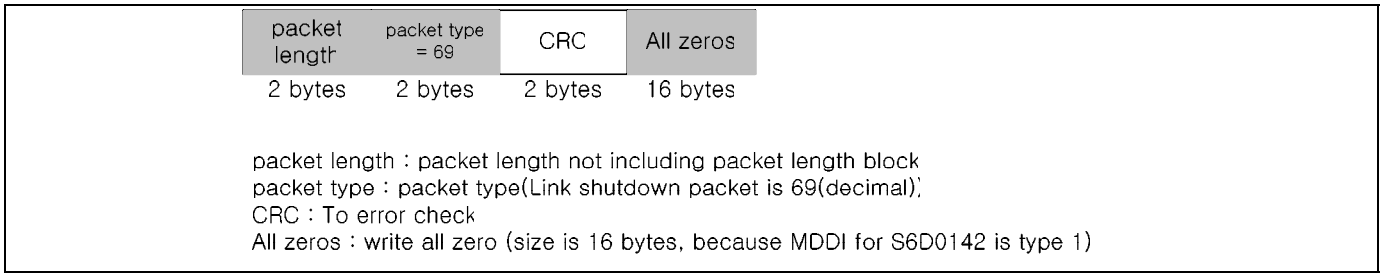


Figure 5.2.6.9.6 Link shutdown packet structure

: fixed value

For More information about MDDI packet, please refer to VESA MDDI spec.

5.2.6.10 MDDI OPERATING STATE

In MDDI, six operation modes are available. The following table describes six modes.

STATE	OSC	Step-up Circuit	Internal Logic status	MDDI I/O	Wake-up by
SLEEP	ON	Disabled	Display OFF MDDI Link hibernation	Hibernation driver ON	Host – Initiated
WAIT	ON	Disabled	Display OFF MDDI Link in SYNC	standard driver ON	-
Normal	ON	Enabled	Display ON MDDI Link in SYNC	standard driver ON	-
NAP	ON	Disabled	Display OFF MDDI Link in SYNC	standard driver ON	-
IDLE	ON	Enabled	Display ON MDDI Link hibernation	Hibernation driver ON	Host – Initiated Client –Initiated (Vsync, GPIO)
STOP	OFF	Disabled	Display OFF MDDI Link OFF	Driver All OFF	RESET

SLEEP: Initial status when external power is connected to the IC.
In this state, internal oscillator is operating, and MDDI link is in hibernation state.
As no command or signal is applied to the IC except RESET input, internal logic or step-up circuit is OFF.

WAIT: After the wake-up sequence, the IC is in WAIT state. MDDI link is in SYNC, and internal logic or step-up is still OFF because no other register access or video stream packet is transferred to the IC.

NORMAL: MDDI link, step-up circuit, and internal logic circuit is ON. Register access or Video data transfer is available in NORMAL state.

IDLE: When no more video data update is needed, MDDI link is in hibernation so that interface power can be reduced. Internal step-up & logic circuits are still operating. MDDI link wakeup will be accomplished when vsync wakeup register is set before hibernation or GPIO interrupt is set.

NAP: This state is set by register access. Step-up and Internal logic is OFF, but MDDI link is ON.
MDDI link have to be in SYNC because the IC must receive commands for power save or normal operation

STOP: STOP state is set by register access (R10h). In this state, MDDI link, internal oscillator, step-up, and logic circuit are all OFF. To release STOP state, input reset signal. After reset, status is SLEEP state.

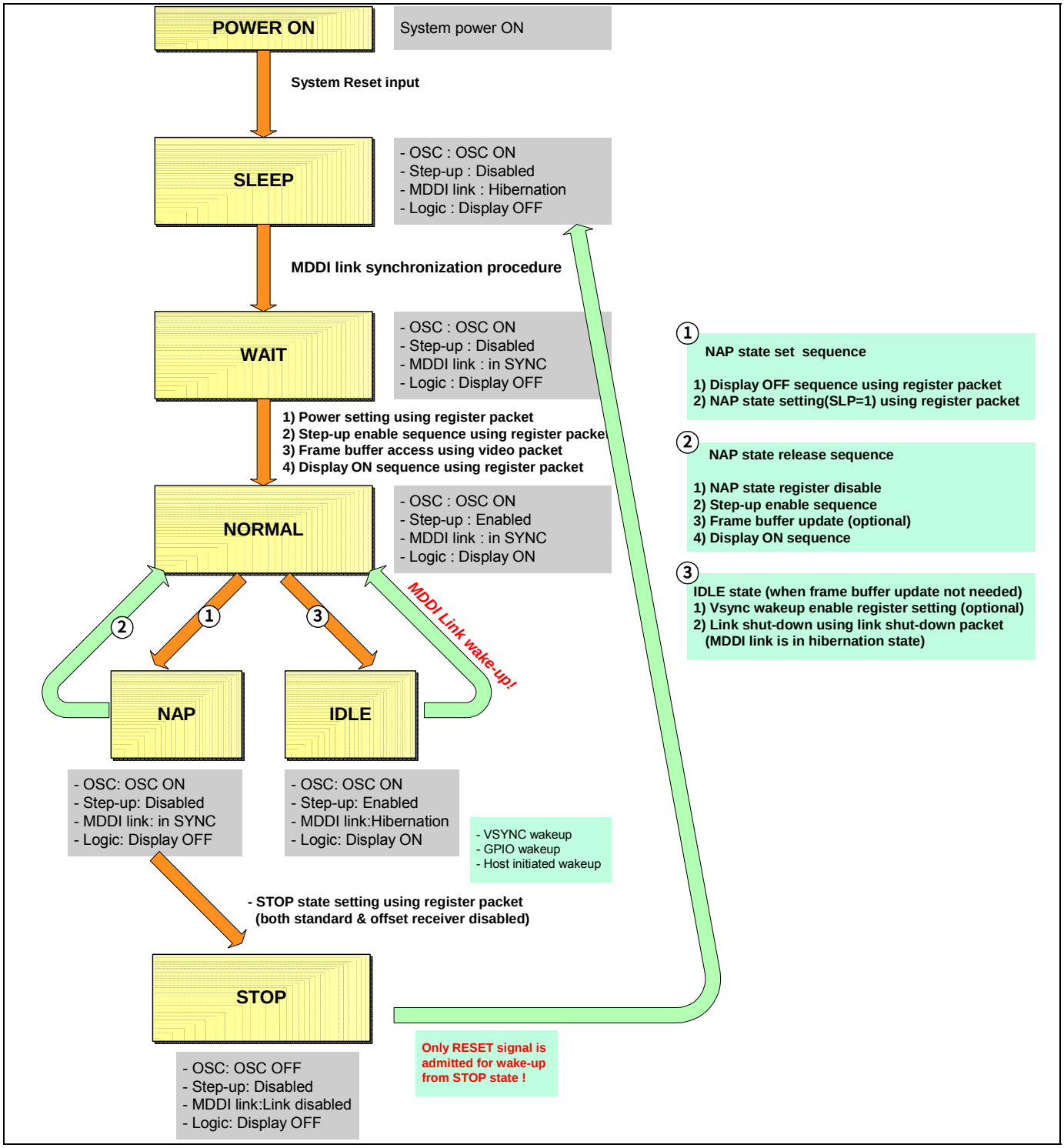


Figure 5.2.6.10.1 Operating state in MDDI mode

5.2.6.11 TEARING LESS DISPLAY

In S6D1121, the matching between data writing timing and written data display timing is important. If timing is mismatched, tearing effect can occur. To avoid display tearing effect, two possible ways are suggested. First case is that data write is slower than speed of displaying written data. In this case, data write speed is not critical, but current consumption in interface will be increased because data transfer time is long. Data write time is selected widely in this case. Other case is that data write is faster than speed of displaying written data. In this case, data update speed is very high so that transfer time is short. So current consumption in interface can be minimized, but it requires fast data transfer. The most important thing is to avoid data scan conflicts with data update. The following figures describe some examples to avoid display tearing phenomenon.

Display speed is faster than data write:

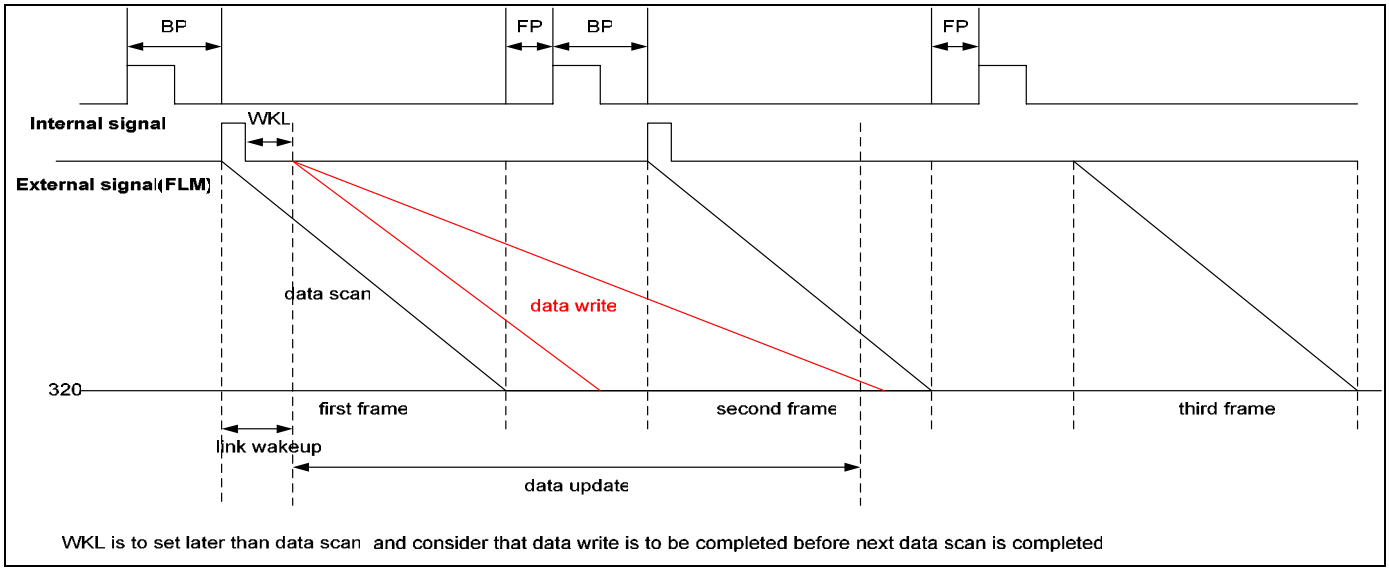


Figure 5.2.6.11.1 Tearing-less Display: Display speed is faster than data write

Display speed is slower than data write:

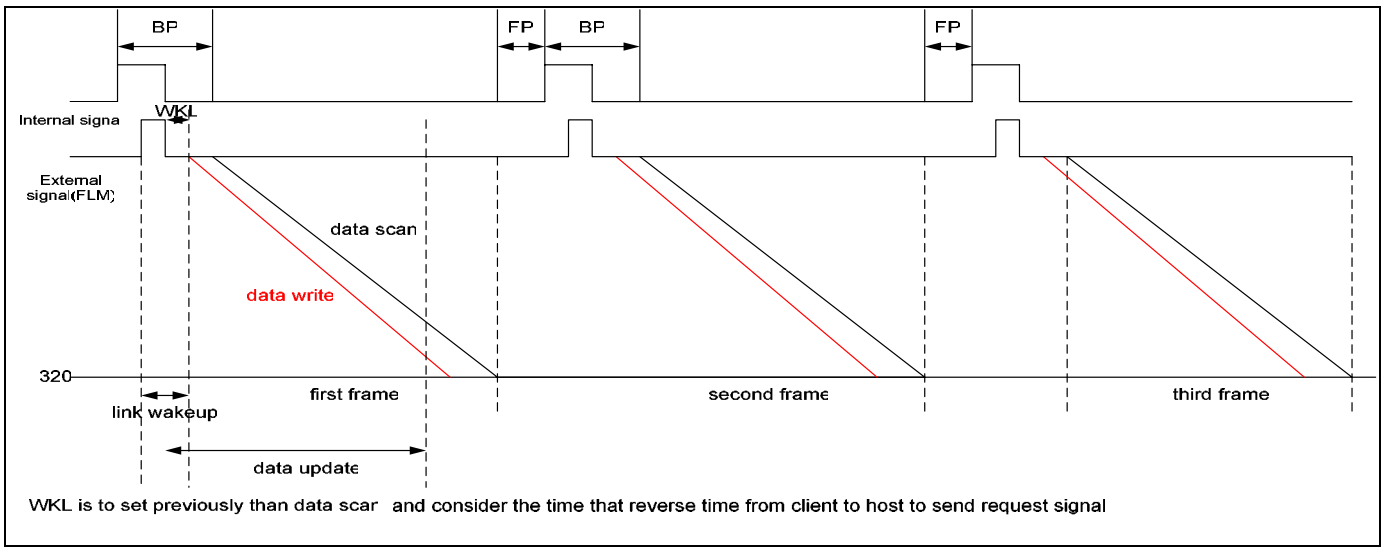


Figure 5.2.6.11.1 Tearing-less Display: Display speed is faster than display

5.2.7 SUB PANEL CONTROL ON MDDI

S6D1121 supports a sub panel control function which controls sub panel driver IC using 68-/80-mode protocol (CSB, RS, RW_WRB and DB). Also supports on 80-mode protocol of STN type. When MDDI host (Base band modem) sends several packets to S6D1121, if the packet is for sub panel, the IC converts the packet to 68-/80-mode protocol and sends them to sub panel driver IC. So separated line for sub panel control are not needed. After all, S6D1121 enables the sub panel driver IC which doesn't support MDDI to be applied to the system. S6D1121 supports only 68-/80-mode 18/16/9/8 bit format for sub panel control.

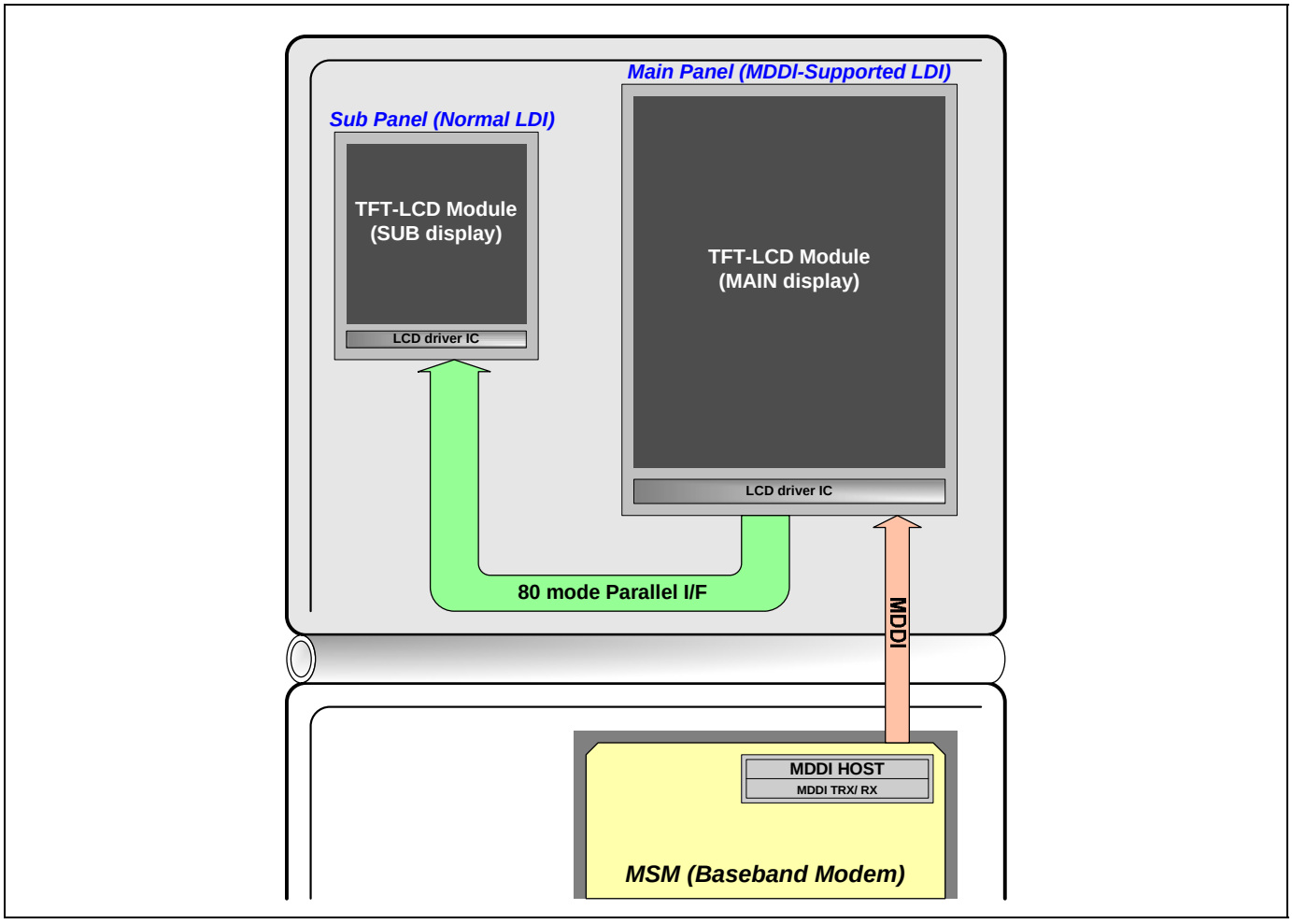


Figure 5.2.7.1 Schematic Diagram of Sub Panel Control Function

5.2.7.1 MAIN / SUB PANEL SELECTION

Using 53h register (53h address can be changed using SUB_SEL register), main / sub panel data path can be selected. When S6D1121 receives register access packet (Initially 53h index) from MDDI host, it decodes the packet and checks the last bit of the register data field is '1' or '0'. If the last bit is '0', the following register access packet or video stream packet is transferred to the sub panel control signal generation block.

Sub panel selection address (Initially 53h) can be changed using SUB_SEL register. Do not change the SUB_SEL value to previously occupied address.

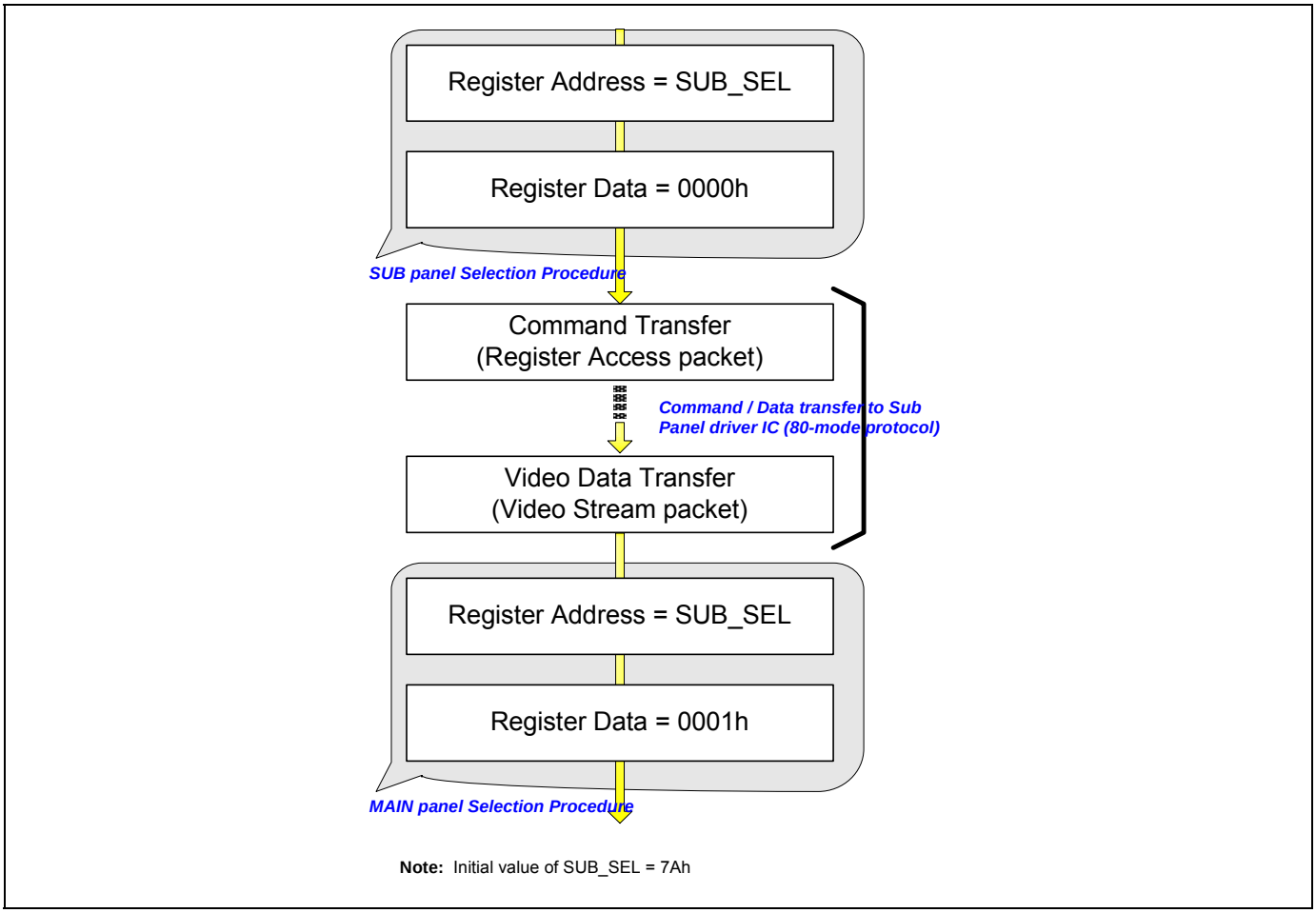


Figure 5.2.7.1.1 Main / Sub panel selection procedure

When video data is transferred to the sub panel driver IC via S6D1121, additional GRAM access command (normally 22h on the Sub Panel Driver IC) is automatically generated in S6D1121.

5.2.7.2 SUB PANEL TIMING

5.2.7.2.1 TFT TYPE SUB PANEL TIMING

Register Data Transfer Timing:

If sub panel is selected, and sub panel type is TFT, register setting is executed like below figure. Register data is transferred through S_DB [17:10] and S_DB [8:1] in 18/16 bit type. If 9/8 bit type is used, data is transferred thorough S_DB [17:10]. Refer to sub panel control (15h index) section.

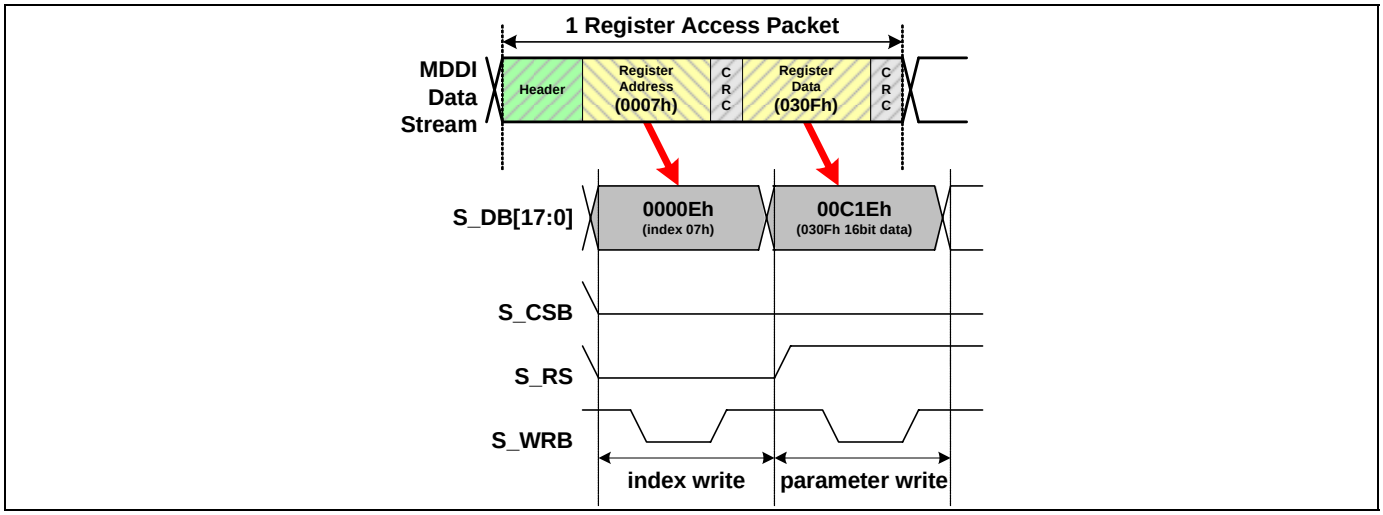


Figure 5.2.7.2.1.1 18/16 bit type register access data transfer

In 9/8 bit mode, S_DB [17:10] is used. In this mode, data is transferred at two times. First transfer is MSB 8bit and second transfer is LSB 8bit.

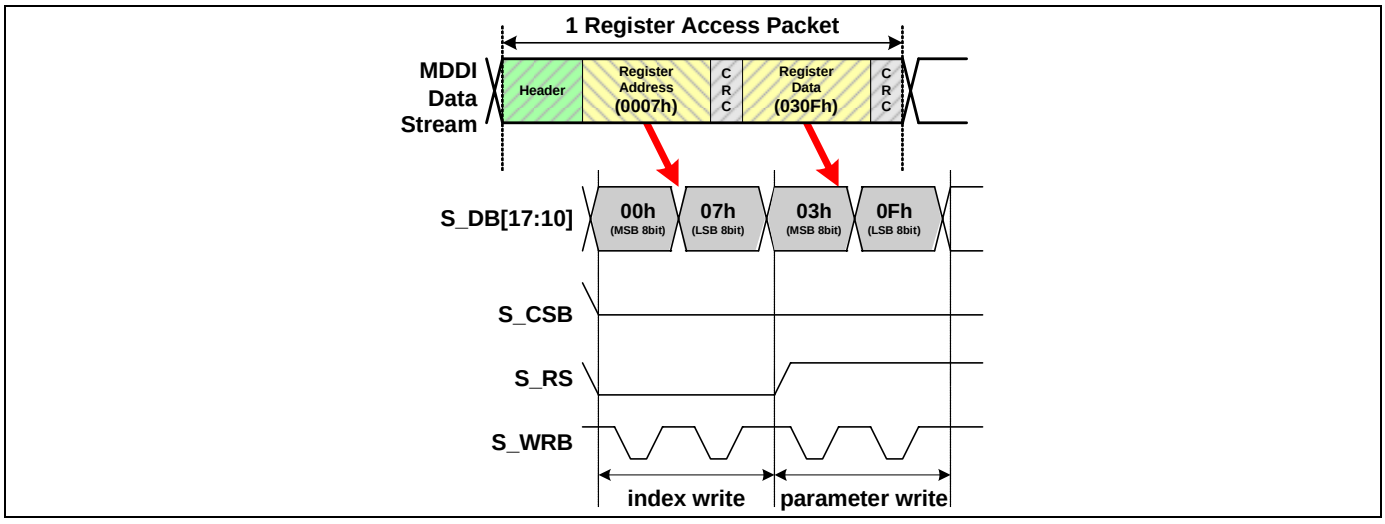


Figure 5.2.7.2.1.2 9/8 bit type register access data transfer

This figure shows register setting timing of 18/16 bit on the 68 mode. In the 68 mode, S_WRB must be connected to E_RDB of sub panel module. RW_WRB of sub panel module must be tied to VSS. Only S6D1121 writes data to sub panel module.

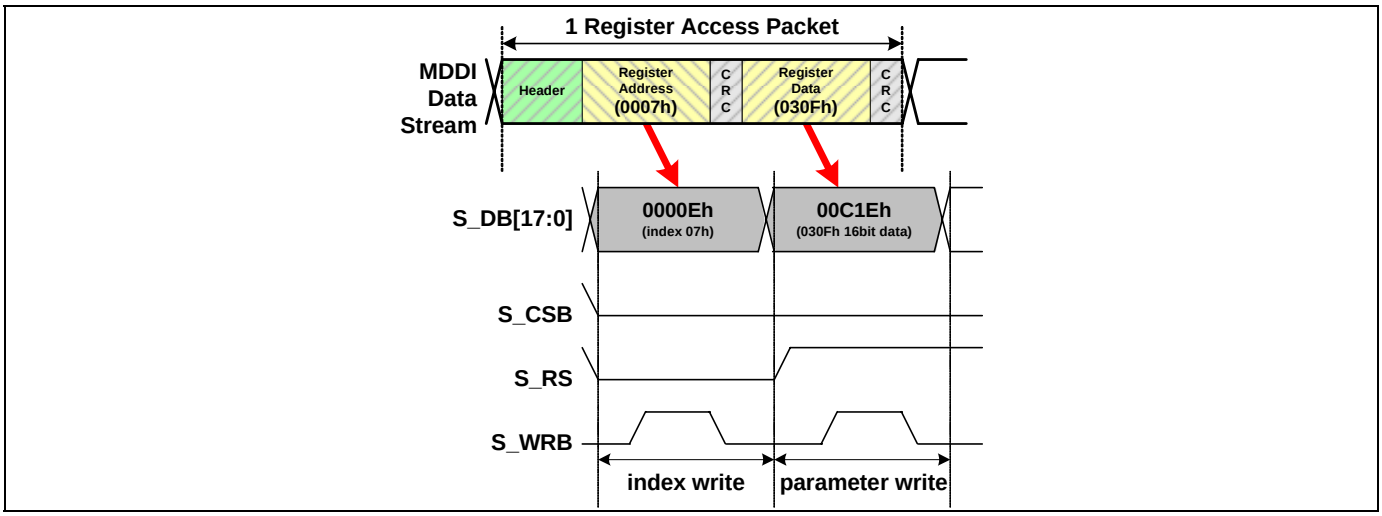


Figure 5.2.7.2.1.3 68 mode 18 bit register data transfer

Video Data Transfer Timing:

In the TFT type sub panel, STN_EN register in 15h index is “0”, and if user wants to use 68-mode interface protocol, then MPU_MODE is set to “1”. 18/16/9/8 mode is selected as setting SUB_IM register. Refer to 15h index description.

This figure shows the 18 bit Video data transfer on the 80 mode.

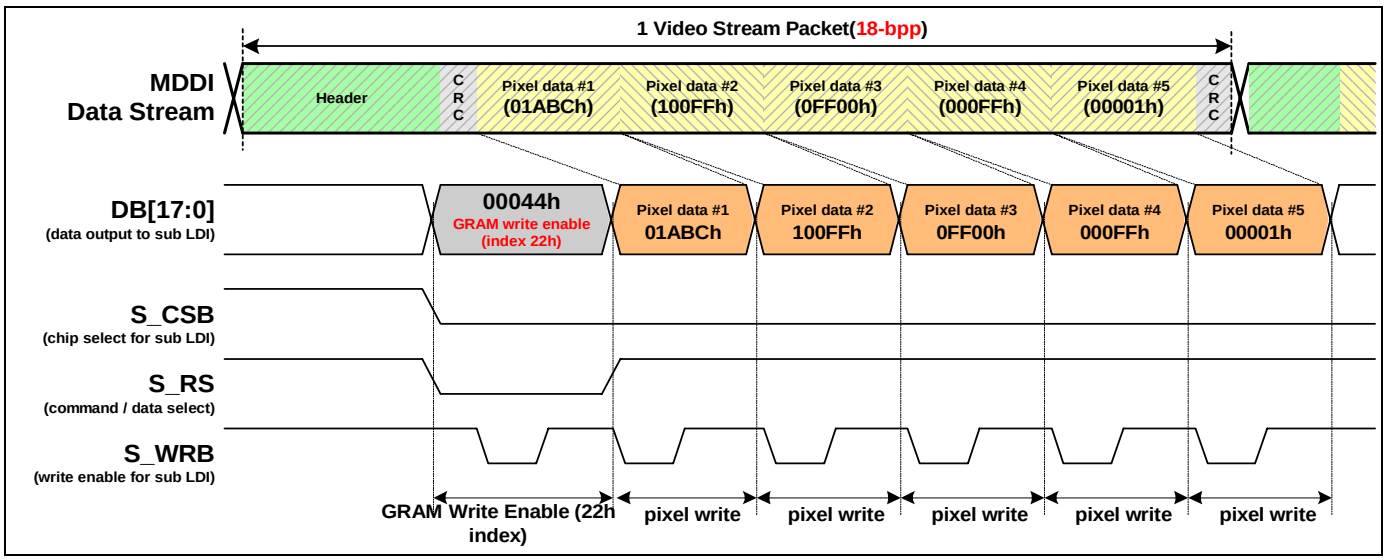


Figure 5.2.7.2.1.4 80 mode 18 bit video data transfer

This figure shows the 18 bit on the 68 mode, S_WRB must be connected to E_RDB of sub panel module. RW_WRB of sub panel module must be tied to VSS. Only S6D1121 writes data to sub panel module.

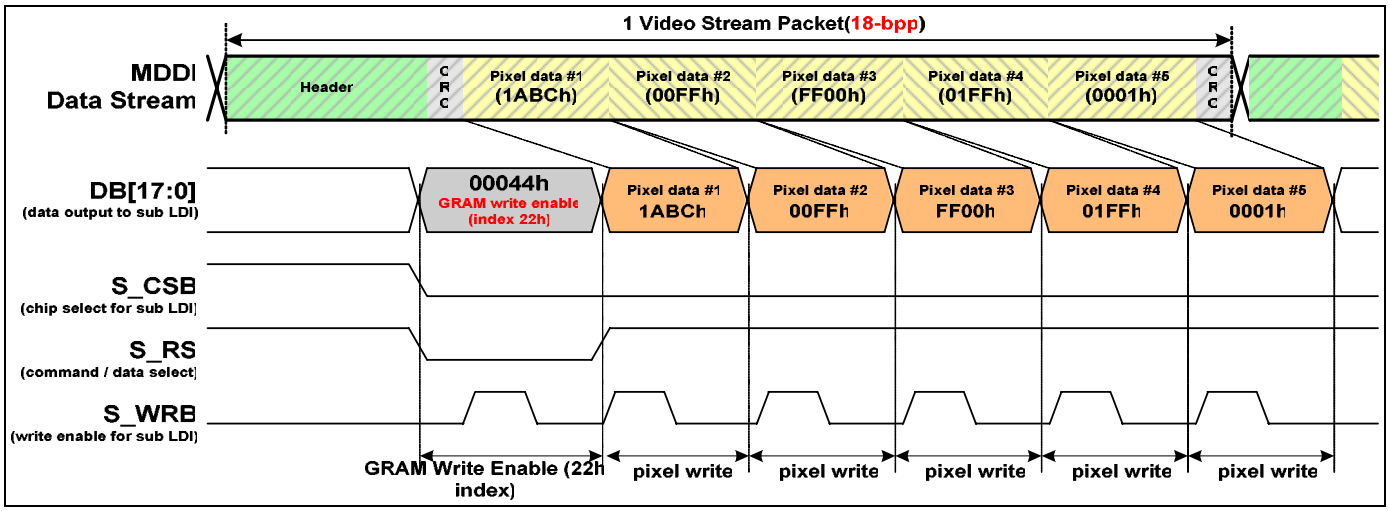


Figure 5.2.7.2.1.5 68 mode 18 bit video data transfer

This figure shows 80-mode 16 bit Video data transfer.

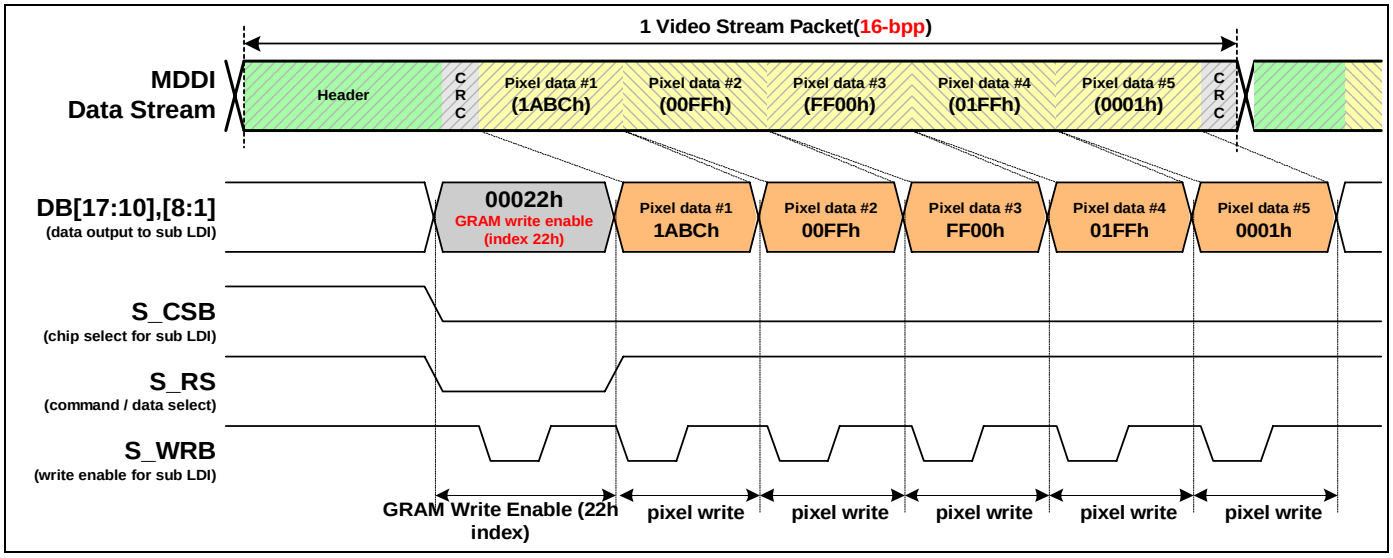


Figure 5.2.7.2.1.6 80 mode 16 bit video data transfer

This figure shows 80-mode 9 bit Video data transfer.

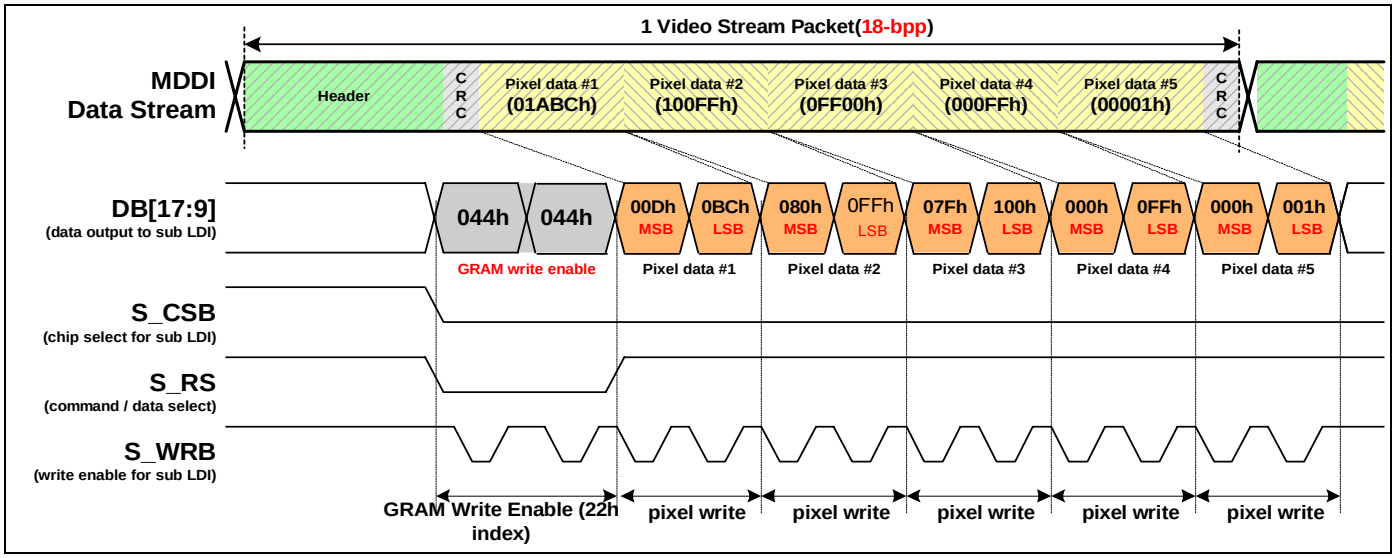


Figure 5.2.7.2.1.7 80 mode 9 bit video data transfer

This figure shows 80-mode 8 bit Video data transfer.

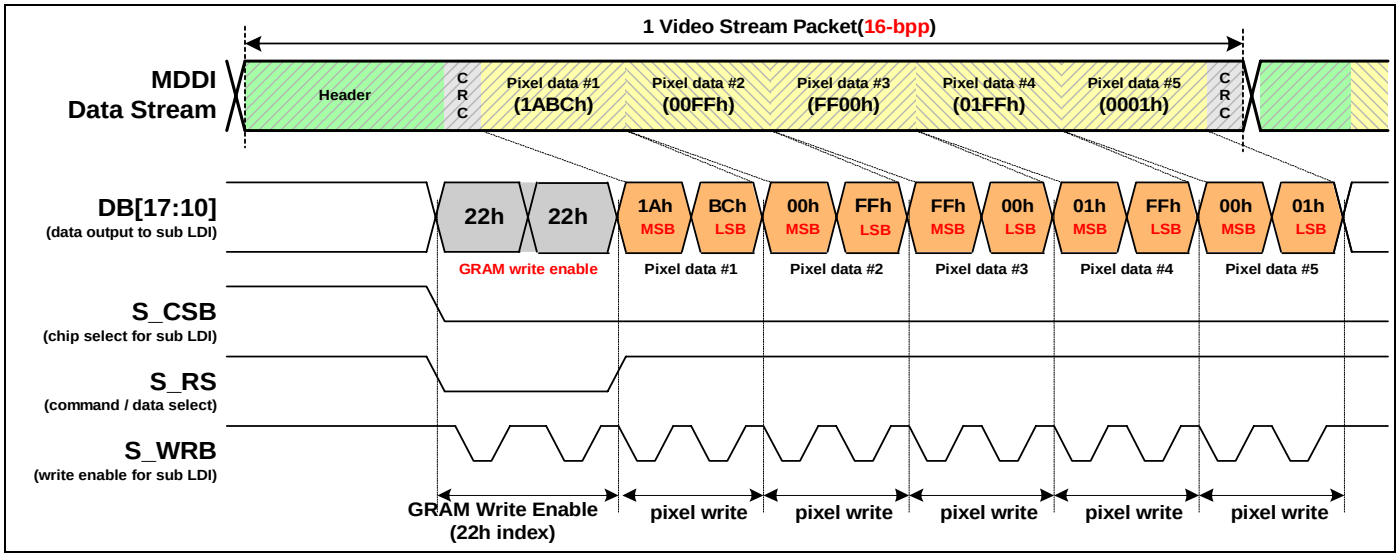


Figure 5.2.7.2.1.8 80 mode 8 bit video data transfer

5.2.7.2.2 STN TYPE SUB PANEL TIMING

Register Data Transfer Timing:

This figure shows conventional type STN mode register data setting. Conventional type does not include parameter.

Instruction type is only 8bit. To use STN type, STN_EN is set to “1”. In STN type, S6D1121 controls S_RS pin using register address [0] in register access packet. Register address [0] is “0”, then S_RS is set to “0”, and register address [0] is “1”, S_RS is set to “1”. Refer to sub panel control (15h index) section.

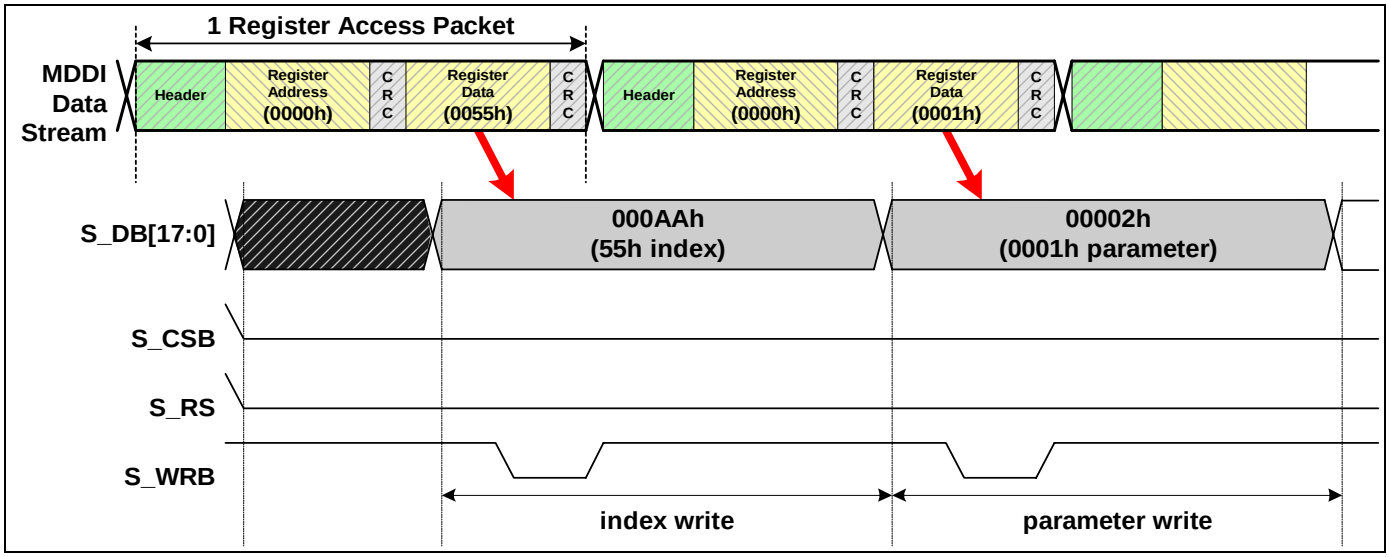


Figure 5.2.7.2.2.1 80 mode STN type conventional register instruction

This type is used to include parameter. When instruction is transferred, S_RS is zero, and when parameter is transferred, S_RS is “1”. S_RS is controlled using register address [0] of register access packet.

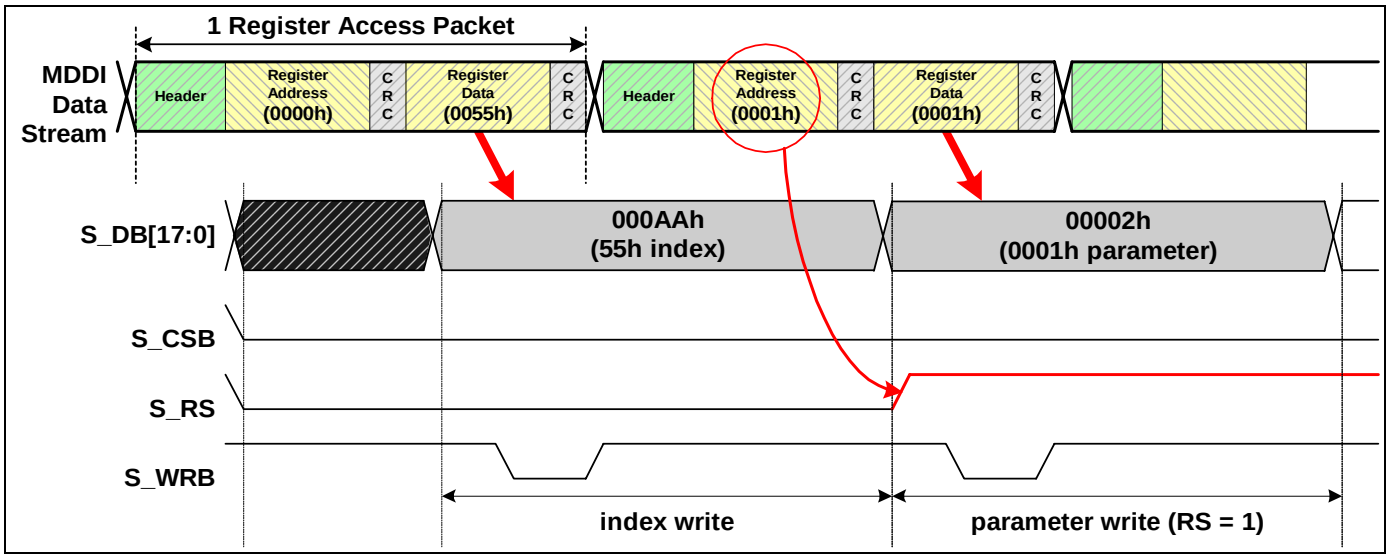


Figure 5.2.7.2.2.2 80 Mode STN Type Included Parameter

Video Data Transfer Timing:

In STN mode, video data start register (like 22H is TFT mode) does not need generally. But some STN type needs video data start register. If those types of STN DDI are used, user has to set the register index. This figure shows STN 16 bit mode video data transfer.

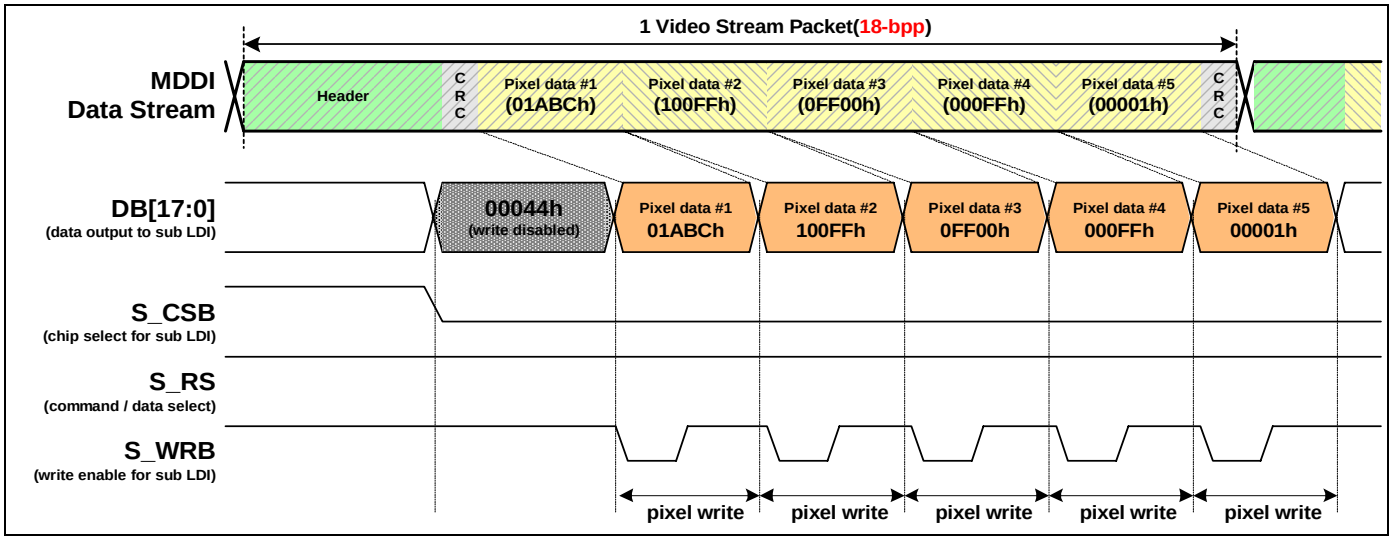


Figure 5.2.7.2.2.3 80 mode STN type 16 bit Video Data Transfer

This figure shows STN 8bit mode video data transfer. If STN video data is 16bit mode, data transfer is executed during 2 times. Fist transfer is MSB 8bits, and second is LSB 8bits.

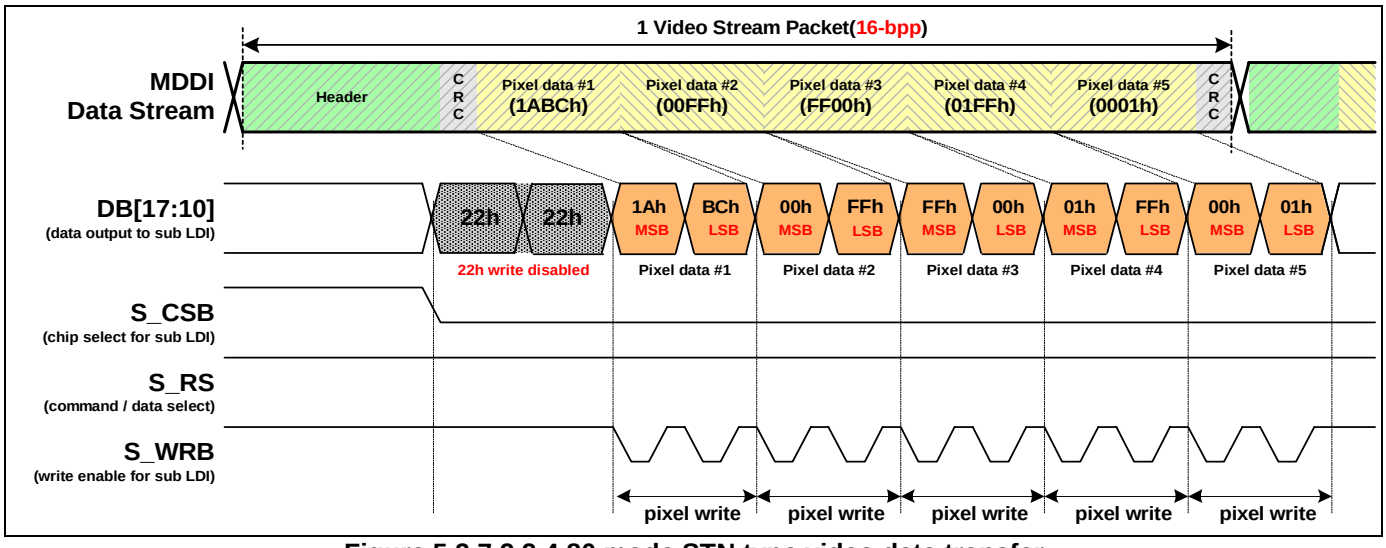


Figure 5.2.7.2.2.4 80 mode STN type video data transfer

5.2.7.2.3 CHANGE DATA PATH FROM SUB PANEL TO MAIN PANEL

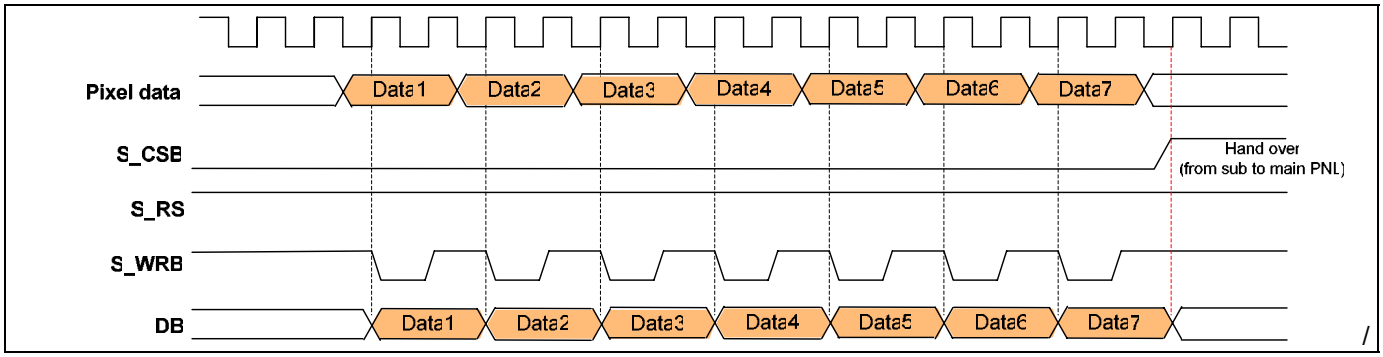


Figure 5.2.7.2.3.1 Handover Timing from Sub Panel to Main Panel

5.2.7.3 MDDI INTERGRATED SYSTEM STRUCTURE

MDDI support display system which incorporates GPIO and Sub panel control is seen below.
S6D1121 can display to a maximum of QVGA (240x320) resolution and sub panel resolution can be chosen according to the system requirement.

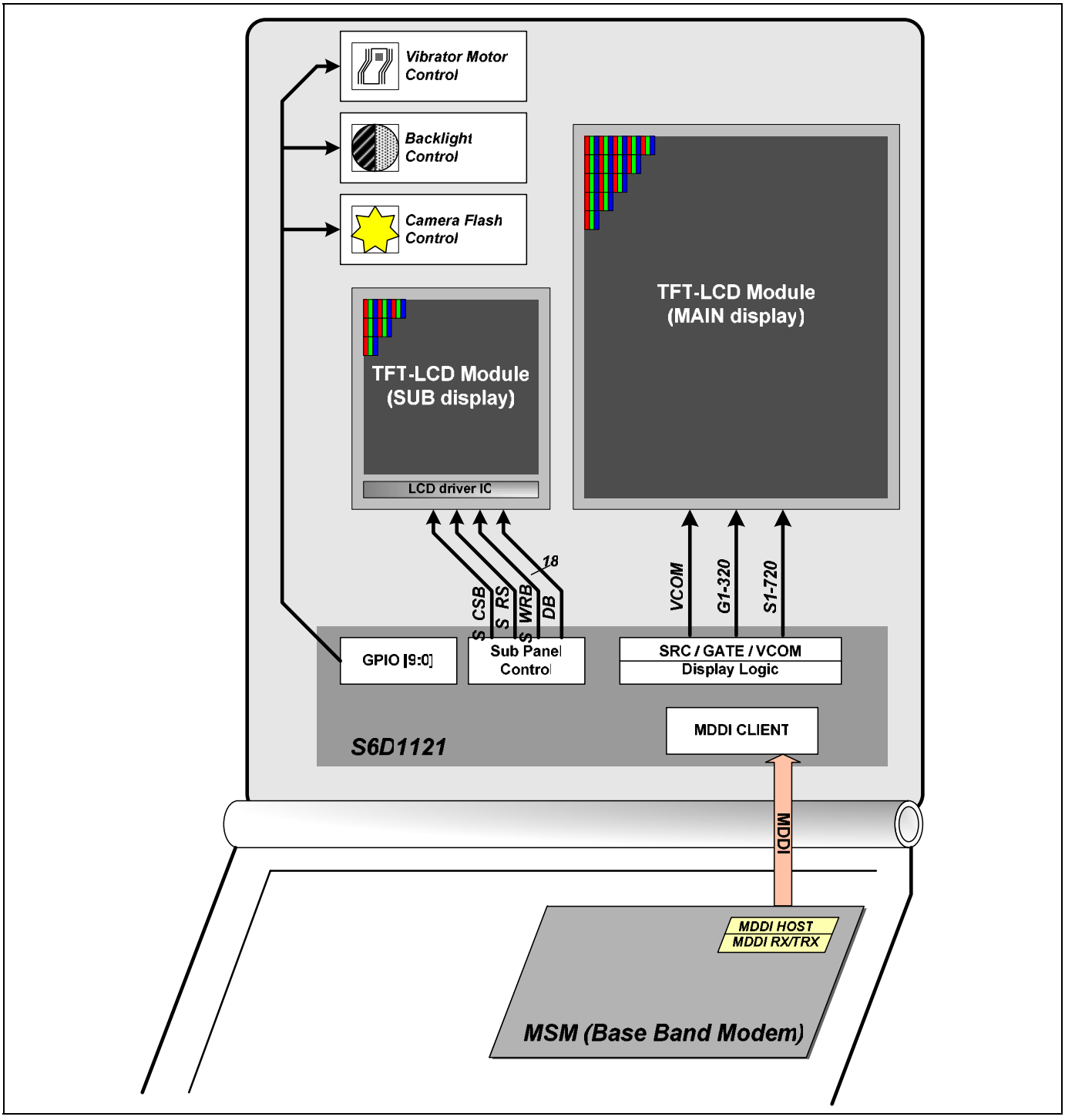


Figure 5.2.7.3.1 MDDI-Integrated System Structure

5.3 LTPS DISPLAY TIMING GENERATOR

The display timing generator generates the timing signals for the internal timing of the source driver and for the panel gate.

5.3.1 1-LINE PERIOD TIMING

The S6D1121 has two drive systems timing output circuits. Following preparation of these drive system timing are carried out, and a usually different timing signal at the time of a drive a partialness drive is generated.

Table 5.3.1.1 LTPS timing signal information

	Timing Circuit 1/2	Timing @ 70 Hz	Remark
Gate circuit clock signal 1	LGCLK1B, RGCLK1B	43 us	
Gate circuit clock signal 2	LGCLK2B, RGCLK2B	43 us	
Gate circuit clock signal 3	LGCLK3B, RGCLK3B	43 us	
Gate circuit clock signal 4	LGCLK4B, RGCLK4B	43 us	
Gate circuit start pulse signal	LGSPB, RGSPB	43 us	
Multi-plectra switch signal 1	RSWB	10 us	
Multi-plectra switch signal 1	GSWB	10 us	
Multi-plectra switch signal 1	BSWB	10 us	

The clock set up by the oscillator is being used for the clock of one-line period, and it is generating all timing by using 64 clocks as a base. The one-line period is assigning to 64 clocks and is adjusting frame frequency to within a time of the one line period set up by the oscillator.
Moreover, the number of clocks of one-line period can be set up by the one-line period clock setting register (R0Ah).

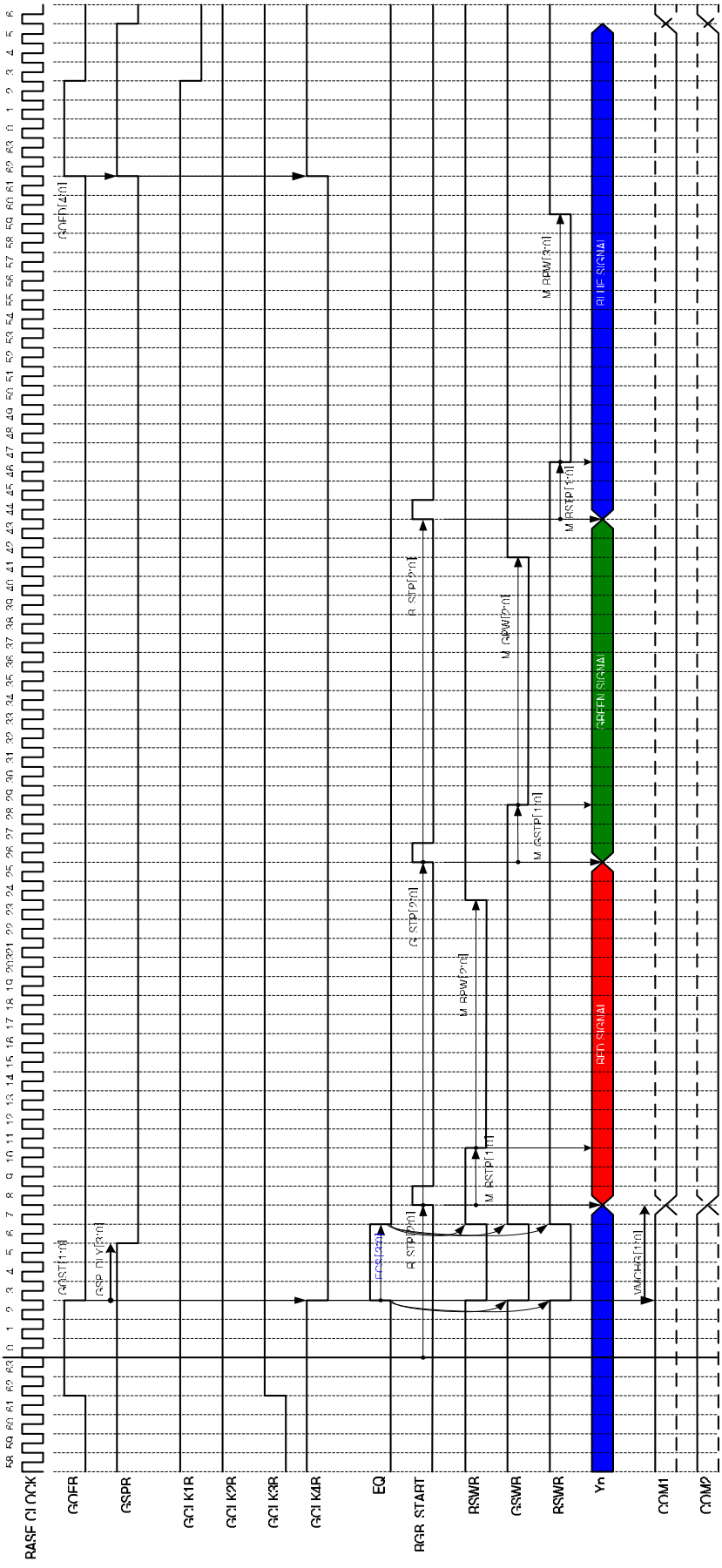


Figure 5.3.1.1 1-Line Driving Period (timing circuit 1, timing circuit 2)

5.3.2 1-LINE PERIOD TIMING IN DEFAULT VALUE

The S6D1121 support the LTPS timing on the default value. The default timing is for 70 Hz. The line depth of 1H is 43 clocks.

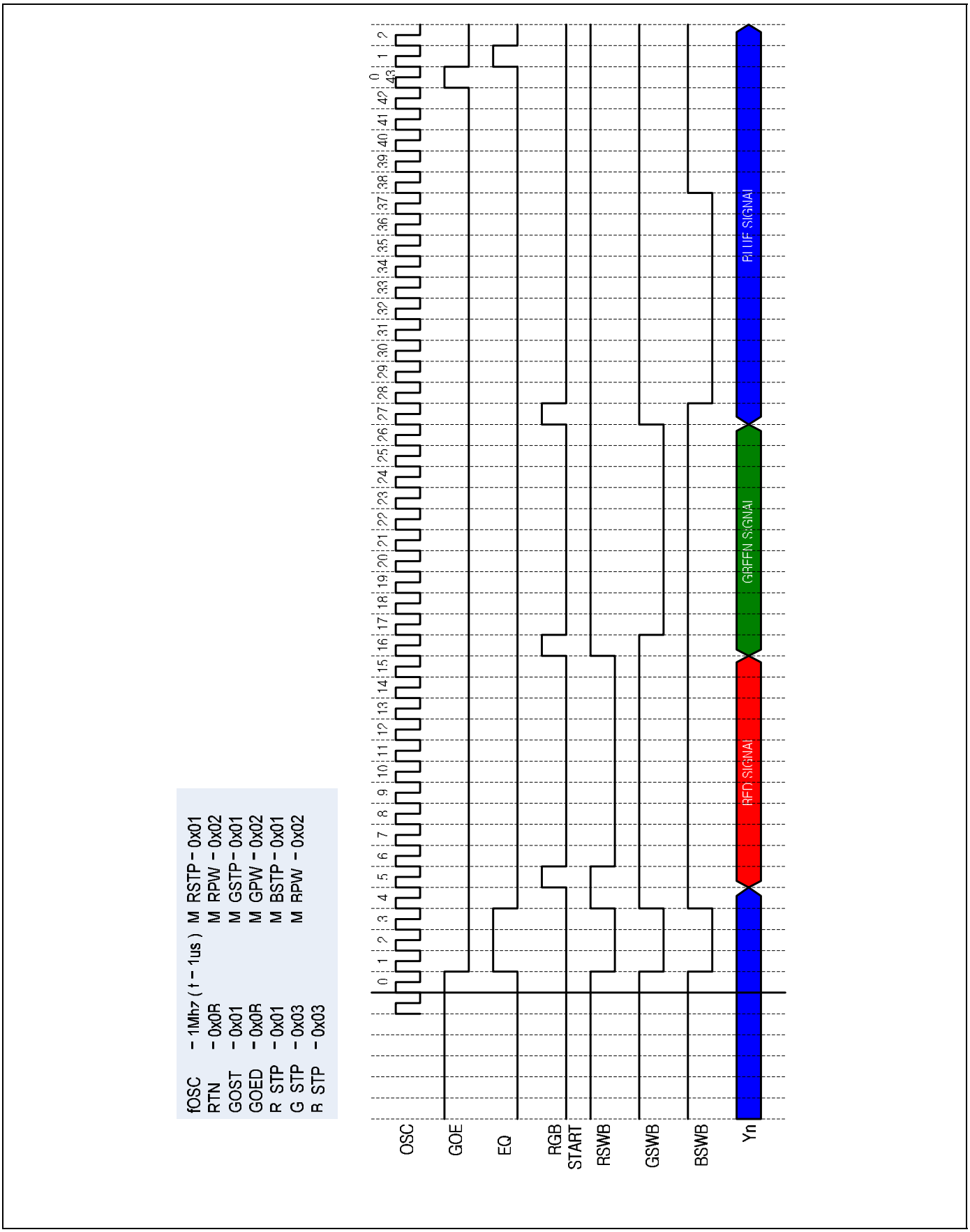


Figure 5.3.2.1 1-Line Driving Period on Default Value (timing circuit 1, timing circuit 2)

5.3.3 1-FRAME PERIOD TIMING

The S6D1121 has two drive systems timing output circuits. Following preparation of these drive system timing are carried out, and a usually different timing signal at the time of a drive a partialness drive is generated. The timing circuit 2 which is a 2 phase gate mode is for the IPS panel. Also, this mode is not needed on the VCOM signal.

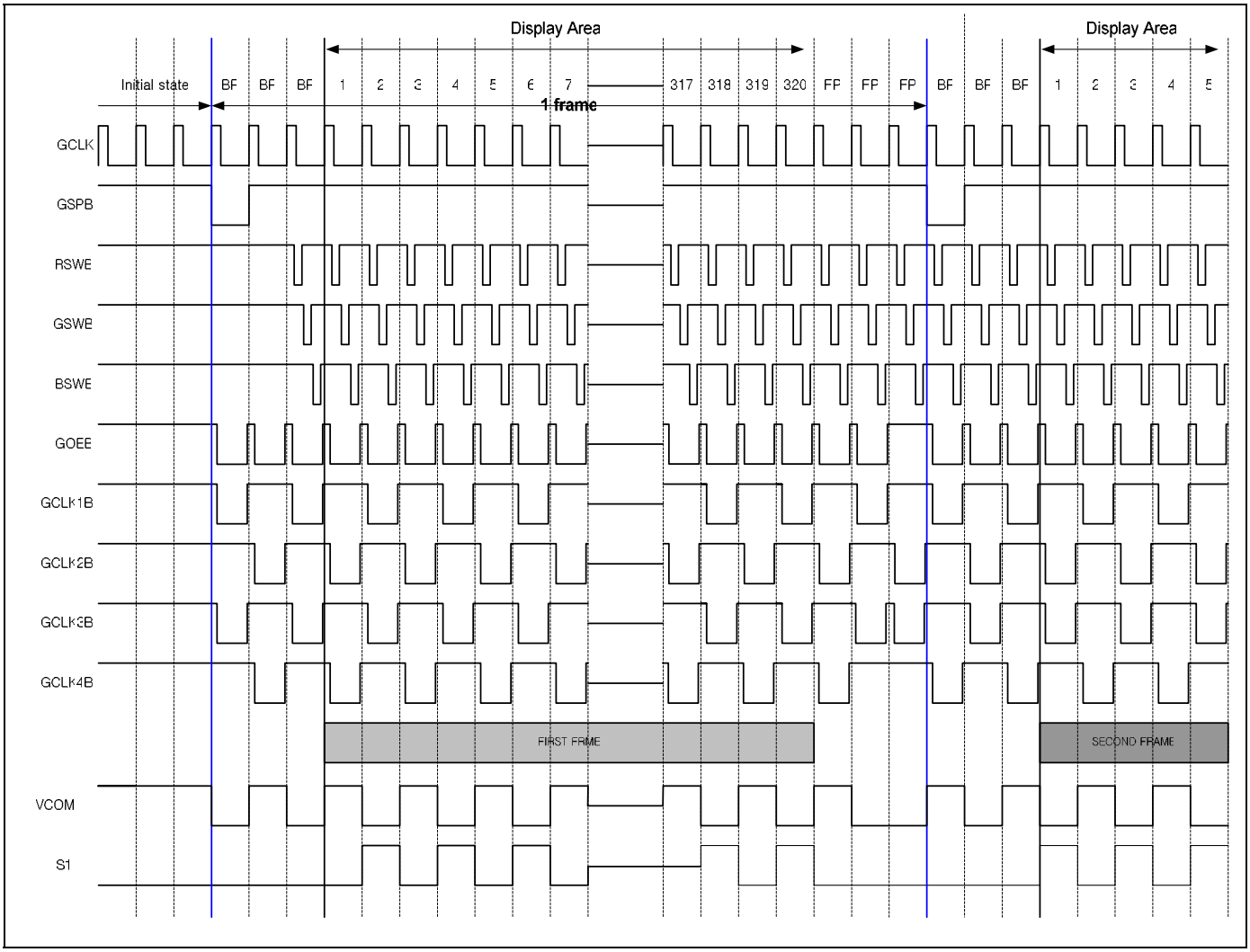


Figure 5.3.3.1 1-Frame Driving Period (timing circuit 2, FLD = 00, BP = 3, FP=3, Black display)

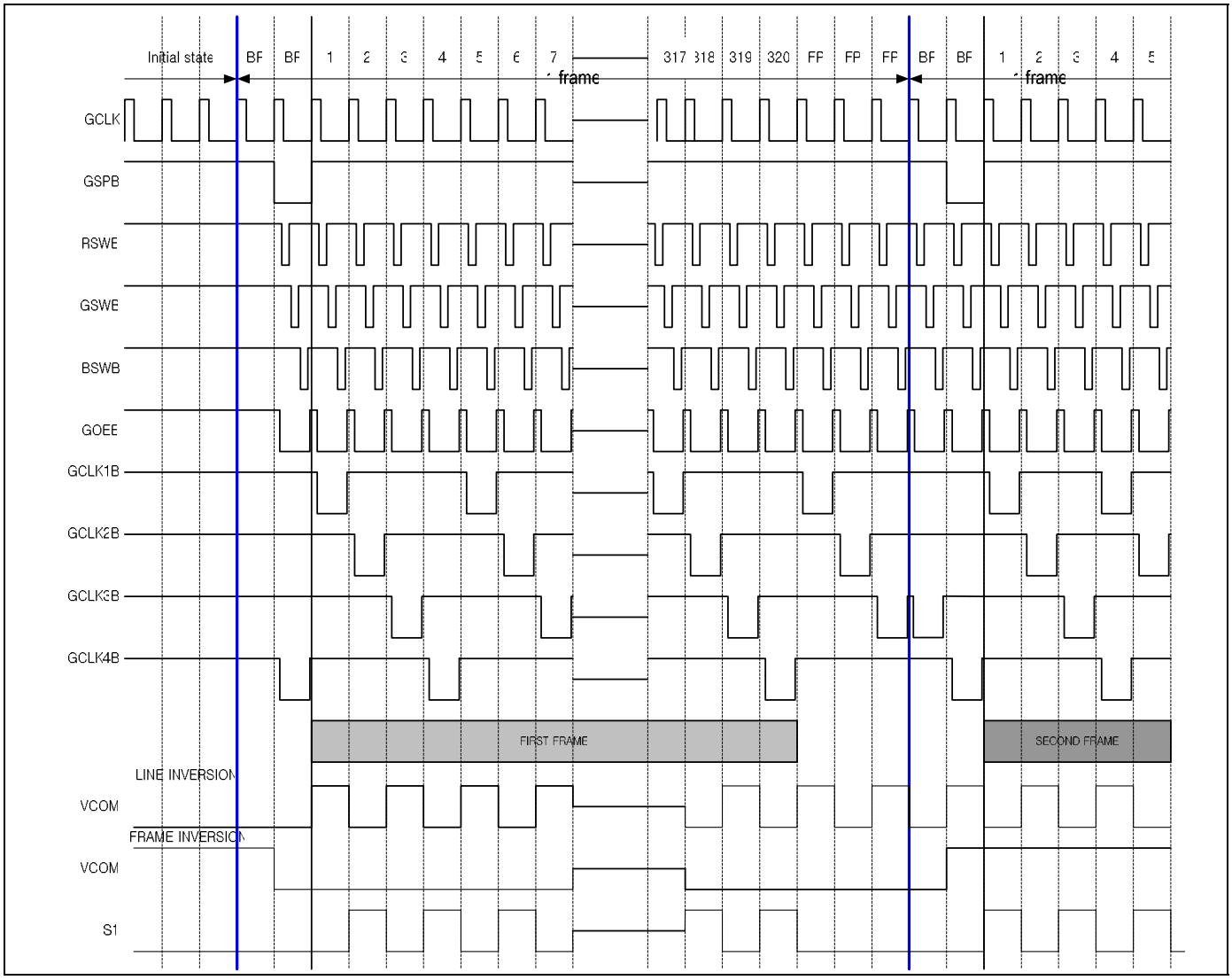


Figure 5.3.3.2 1-Frame Driving Period (timing circuit 1, FLD = 01, FP = 3, BP = 2)

NOTES: Source output is black display and Line inversion with frame inversion (BC = 1, EOR = 1)

5.3.4 1-FRAME PERIOD TIMING OF 2-LINE NORMAL DISPLAY

The S6D1121 has 2-line normal function.

2-line normal mode:
The source output: 1 → 2 → 3 → ……. → 318 → 319 → 320

This function needs at least 6 cycles (FP+BP) between odd frame and even frame. This function only supports on the four phase gate mode (timing circuit 1).

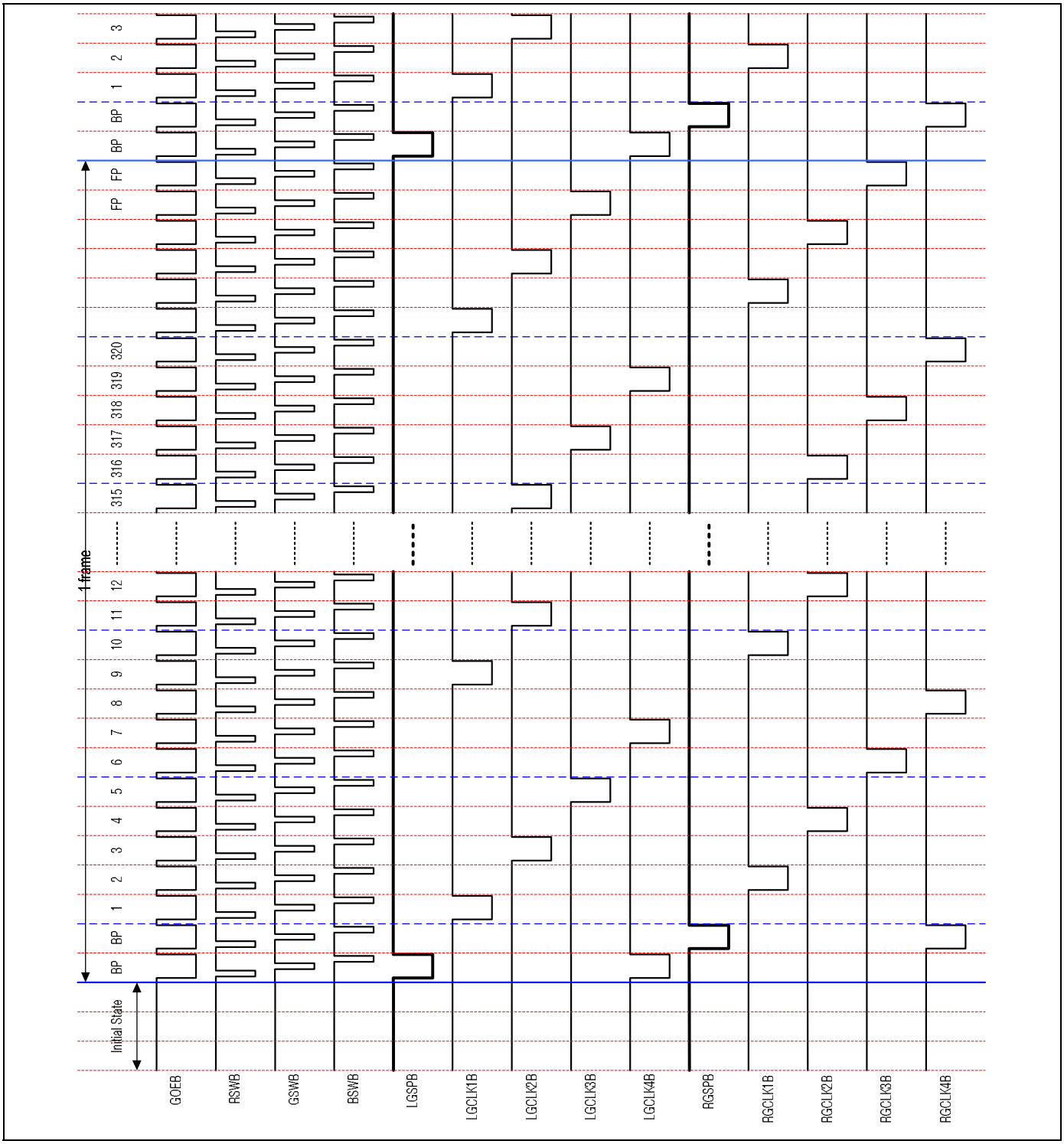


Figure 5.3.4.1 1-Frame Driving Period in 2 Line Normal (timing circuit 1, FLD = 10)

5.3.5 1-FRAME PERIOD TIMING OF 2-LINE INTERLACE DISPLAY

The S6D1121 has 2-line interlace function.

2-line interlace mode:

The even field source output: 2 → 4 → 6 → 8 → ..... → 318 → 320

The odd field source output: 1 → 3 → 5 → 7 → ..... → 317 → 319

There are 4 dummy cycles between odd frame and even frame. This function only supports on the four phase gate mode (timing circuit 1).

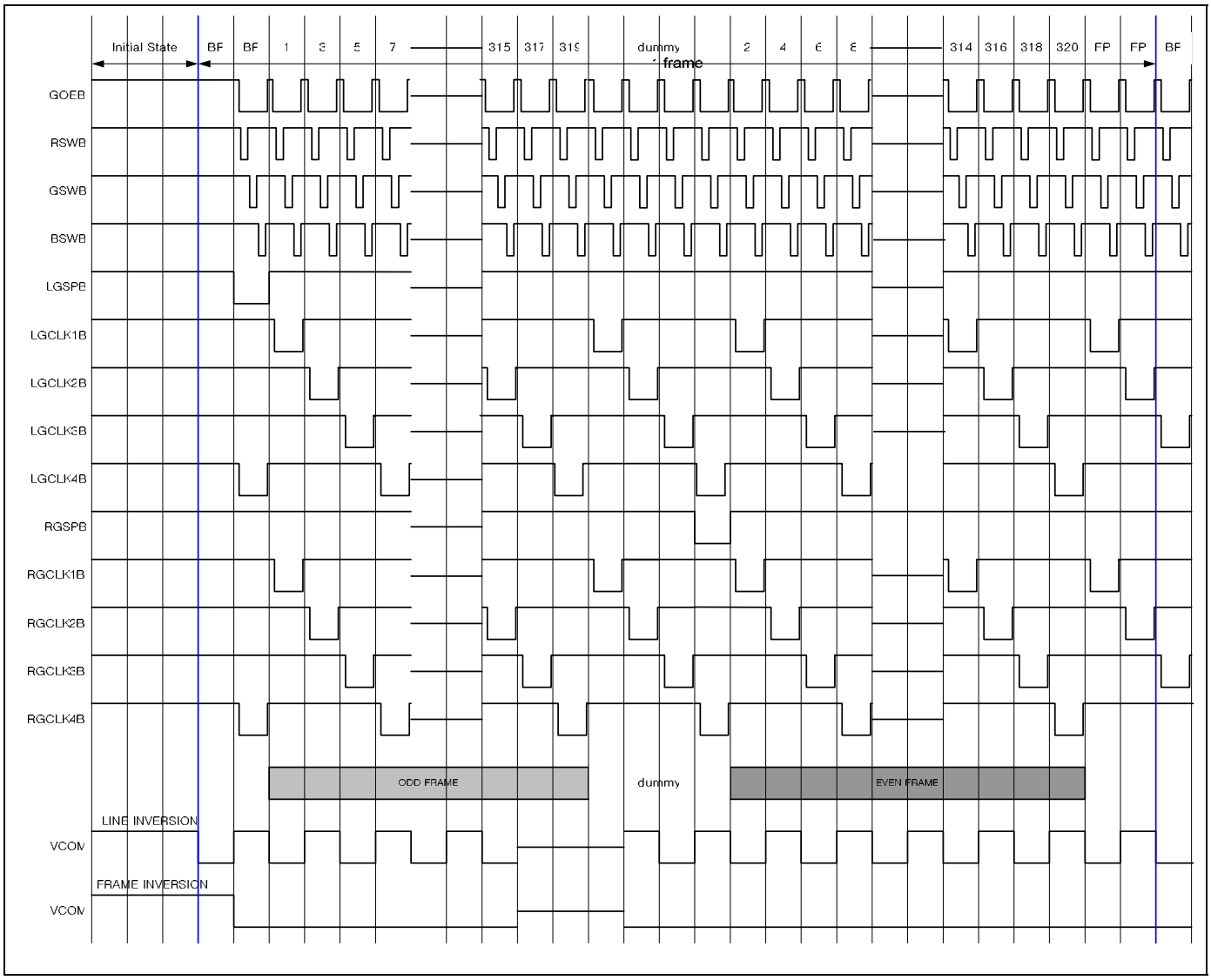


Figure 5.3.5.1 1-Frame Driving Period in 2 Line Interlace (timing circuit 1, FLD = 11)

5.3.6 1-FRAME PERIOD TIMING IN PARTIAL MODE

The S6D1121 supports 4 phase (timing circuit 1) and 2 phase (timing circuit 2) gate types in the partial display mode.

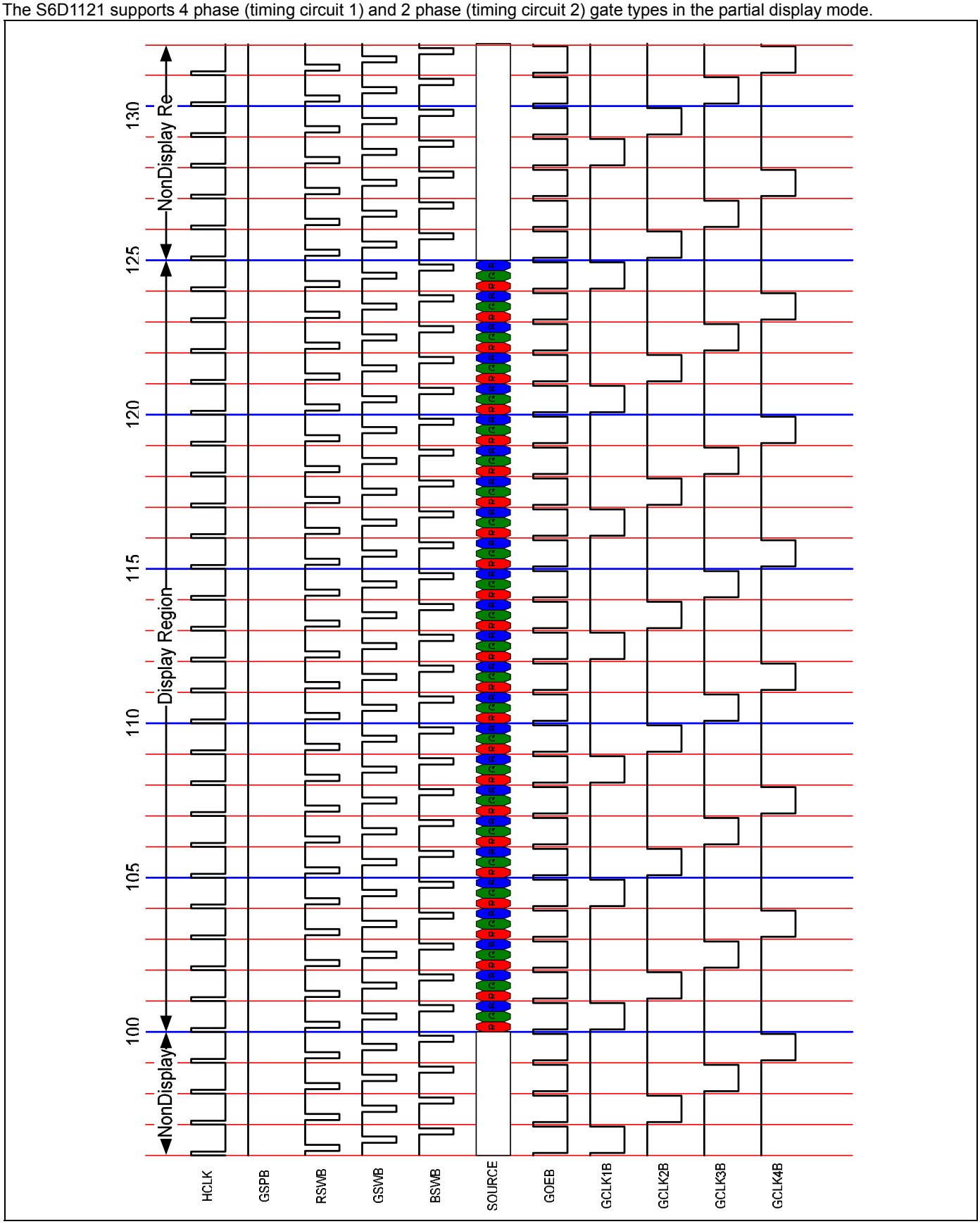


Figure 5.3.6.1 1-Frame Driving Period in Partial Mode (timing circuit 1, FLD = 01)

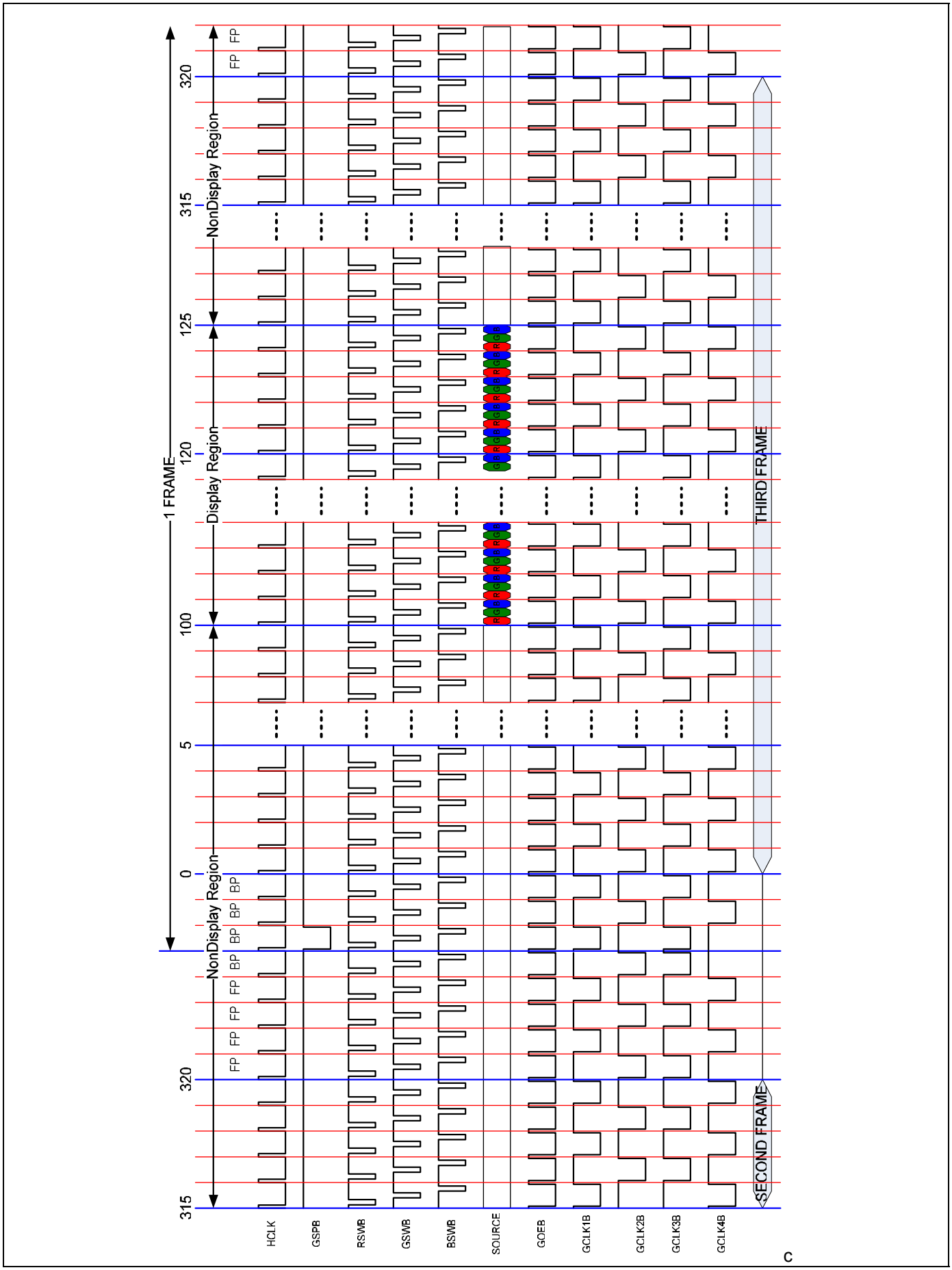


Figure 5.3.6.2 1-Frame Driving Period in Partial Mode (timing circuit 2, FLD = 00)

5.4 DISPLAY FUNCTION

5.4.1 PARTIAL DISPLAY MODE

5.4.1.1 SCREEN-DIVISION DRIVING FUNCTION

The S6D1121 is provided with a function that allows sections within the panel to be displayed separately (partial display mode) .The S6D1121 can select and drive two screens at any position with the screen-driving position registers (R42h/ R43h and R44h/R45h). Any two screens required for display are selectively driven and hence leads to a reduction in LCD-driving voltage and power consumption. For the 1st division screen, start line (SS18 to 10) and end line (SE18 to 10) are specified by the 1st screen-driving position register (R42h/R43h). For the 2nd division screen, start line (SS28 to 20) and end line (SE28 to 20) are specified by the 2nd screen-driving position register (R44h/R45h). The 2nd screen control is effective when the SPT bit is 1. The total count of selection-driving lines for the 1st and 2nd screens must correspond to the LCD-driving duty set value. The address of selection-driving lines for the 1st and 2nd screens must be specified within the NL5-0 register setting value (LCD-driving duty set value).

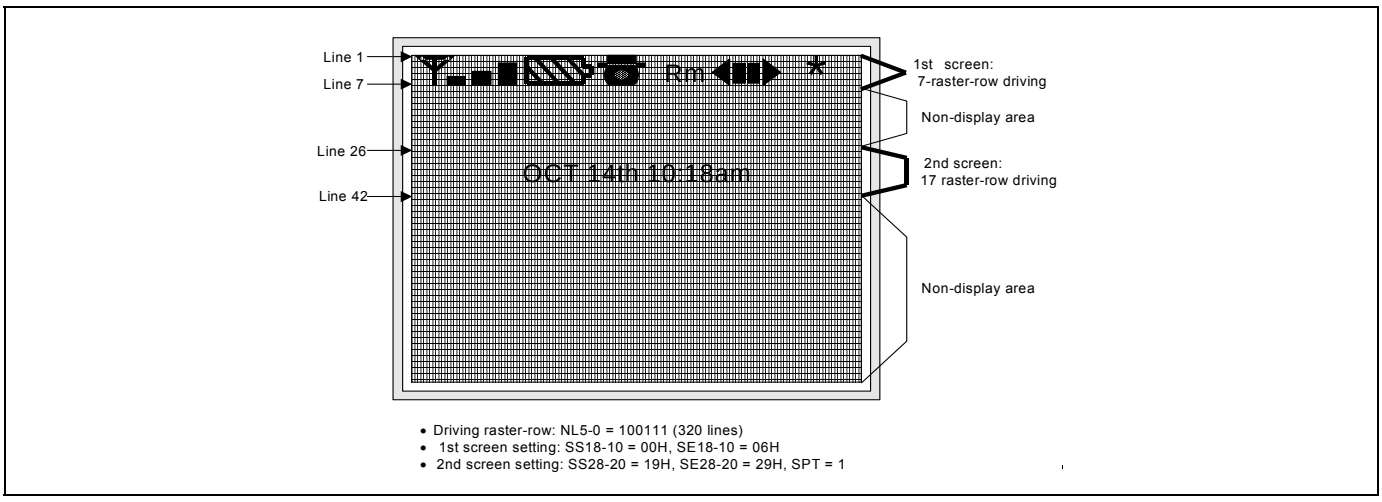


Figure 5.4.1.1.1 Driving on 2 Screens

NOTES:

1. The “scroll step count register” command is ignored in the partial display mode.
2. The specified partial areas must not directly overlap, and the partial 1 area and partial 2 area must be separated by the at least one line. If the areas overlap, only the partial 1 setting are valid, and partial display is not performed for the partial 2 area.
3. The below table is described about the partial and scroll function operation with FLD register.

FLD	Partial Mode/ Scroll mode
00	Operation
01	Operation
10	Operation
11	Not operation

5.4.1.2 RESTRICTION ON THE 1ST/2ND SCREEN DRIVING POSITION REGISTER SETTINGS

The following restrictions must be satisfied when setting the start line (SS18 to 10) and end line (SE18 to 10) of the 1st screen driving position register (R42h/R43h) and the start line (SS28 to 20) and end line (SE28 to 20) of the 2nd screen driving position register (R44h/R45h) for the S6D1121. Note that incorrect display may occur if the restrictions are not satisfied.

Table 5.4.1.2.1 Restrictions on the 1st/2nd Screen Driving Position Register Setting

1st Screen Driving (SPT=0)

Register setting	Display operation
(SE18 to 10) – (SS18 to 10) = NL	Full screen display Normally displays (SE18 to 10) to (SS18 to 10)
(SE18 to 10) – (SS18 to 10) < NL	Partial display Normally displays (SE18 to 10) to (SS18 to 10) White display for all other times (RAM data is not related at all)
(SE18 to 10) – (SS18 to 10) > NL	Setting disabled

NOTES:
1. SS18 to 10 ≤ SE18 to 10 ≤ 13Fh
2. Setting SE28 to 20 and SS28 to 20 are invalid

2nd Screen Driving (SPT=1)

Register setting	Display operation
((SE18 to 10) – (SS18 to 10)) + ((SE28 to 20) – (SS28-20)) = NL	Full screen display Normally displays (SE28 to 10) to (SS18 to 10)
((SE18 to 10) – (SS18 to 10)) + ((SE28 to 20) – (SS28-20)) < NL	Partial display Normally displays (SE28 to 10) to (SS18 to 10) White display for all other times (RAM data is not related at all)
((SE18 to 10) – (SS18 to 10)) + ((SE28 to 20) – (SS28-20)) > NL	Setting disabled

NOTES:
1. SS18 to 10 ≤ SE18 to 10 < SS28 to 20 ≤ SE28 to 20 ≤ 13Fh
2. (SE28 to 20) – (SS18 to 10) ≤ NL

The driver output can't be set for non-display area during the partial display. Decision is based on the specification of the panels.

Refer to the following flow to set up the partial display.

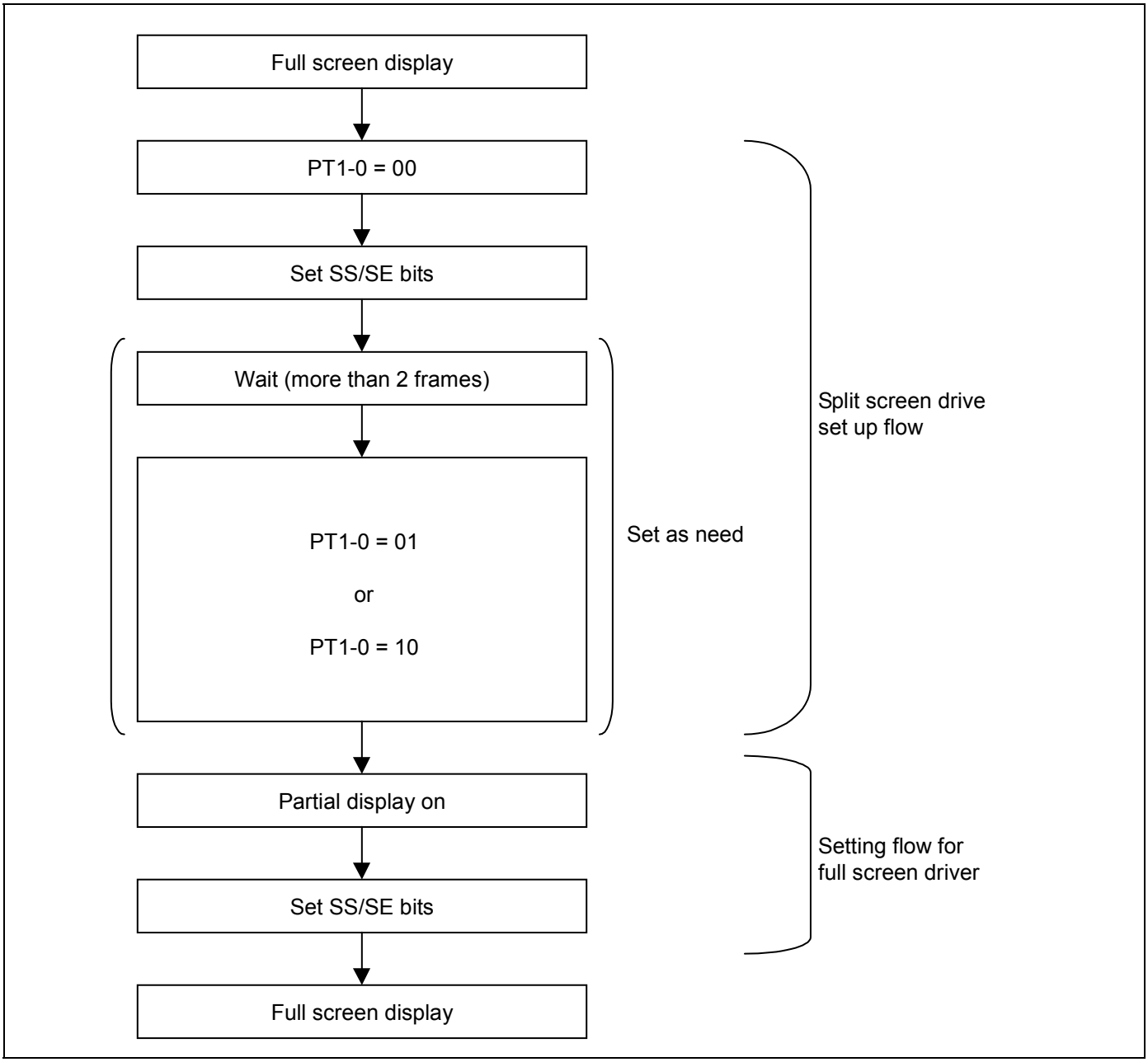


Figure 5.4.1.2.1 Partial display set up flow

5.4.2 PANEL VERTICAL SCROLL MODE

The S6D1121 has a panel scroll function. Any area of the panel can be scrolled by using the scroll area start line register, scroll area end line register, and scroll step count register.

Table 5.4.2.1 Scroll Area Start Line Register (1st Screen Area: SS18 ~ SS10, 2nd Screen Area: SS28 ~ SS20)

SS18	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10	Start Line Vertical address
0	0	0	0	0	0	0	0	0	000H
0	0	0	0	0	0	0	0	1	001H
0	0	0	0	0	0	0	1	0	002H
0	0	0	0	0	0	0	1	1	003H
									↓
1	0	0	1	1	1	1	0	1	13DH
1	0	0	1	1	1	1	1	0	13EH
1	0	0	1	1	1	1	1	1	13FH

Table 5.4.2.2 Scroll Area End Line Register (1st Screen Area: SE18 ~ SE10, 2nd Screen Area: SE28 ~ SE20)

SE18	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	End Line Vertical address
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	0	1	0	3
0	0	0	0	0	0	0	1	1	4
									↓
1	0	0	1	1	1	1	0	1	318
1	0	0	1	1	1	1	1	0	319
1	0	0	1	1	1	1	1	1	320

Table 5.4.2.3 Scroll Step Count Register

VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Scroll Area Line Number
0	0	0	0	0	0	0	0	0	0(No scroll)
0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	1	1	3
									↓
1	0	0	1	1	1	1	0	1	317
1	0	0	1	1	1	1	1	0	318
1	0	0	1	1	1	1	1	1	319

NOTES:
1. SS18 to 10 ≤ SE18 to 10 < SS28 to 20 ≤ SE28 to 20 ≤ 13Fh
2. (SE28 to 20) – (SS18 to 10) ≤ NL

5.4.3 8-COLOR DISPLAY MODE

The S6D1121 incorporates 8-color display mode. The used grayscale levels are V0 and V63 and all the other levels (V1~V62) are halted, so that the power consumption is lowered. During the 8-color mode, the Gamma micro adjustment register, PKP00-PKP52 and PKN00-PKN52 are invalid. The level power supply (V1-V62) is in OFF condition during the 8-color mode in order to select V0/V63.

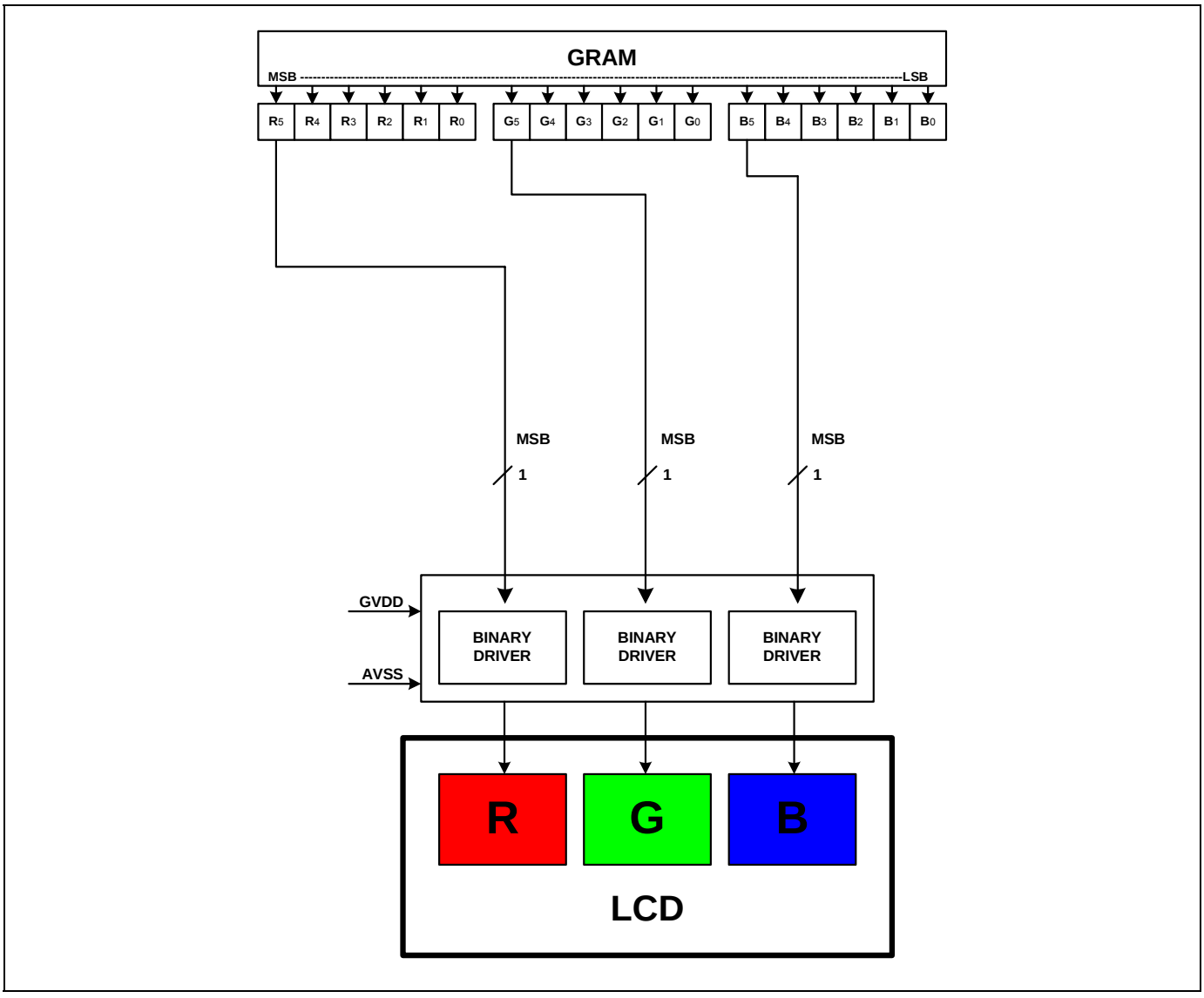


Figure 5.4.3.1 8-color display control

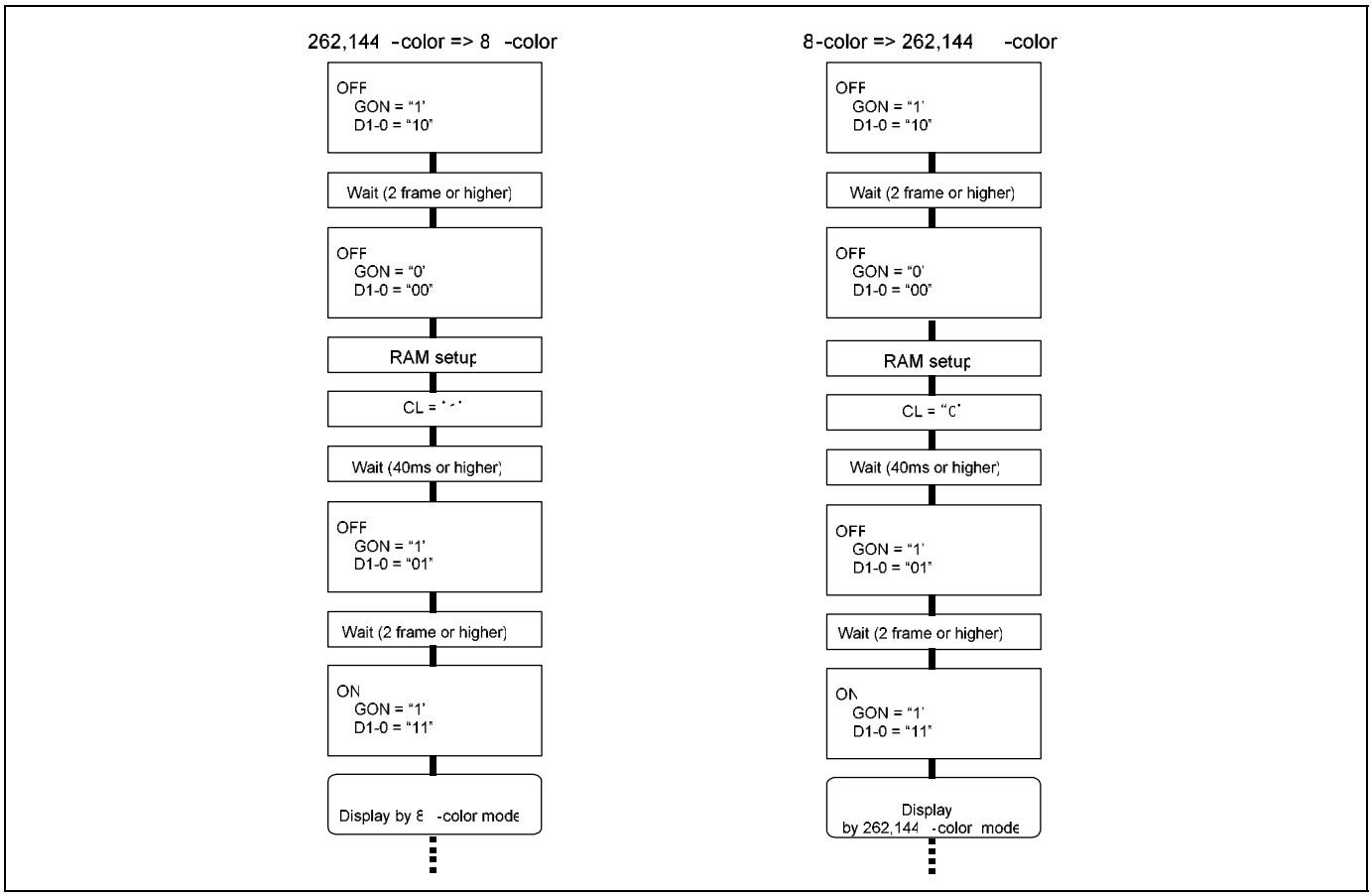


Figure 5.4.3.2 Set up procedure for the 8-color mode

5.5 DISPLAY DATA RAM

5.5.1 HORIZONTAL / VERTICAL ADDRESS

This RAM stores pixel data for display and consists of 4,320 bits (240x18) x 320 bits. Any address of this RAM can be accessed by specifying an Horizontal address and a Vertical address. Display data RAM construction refers to Figure 5.5.1.

Horizontal address circuit:

The horizontal address of the display data RAM is specified by using the horizontal address register (R20h) as shown in Figure 5.5.1. The specified horizontal address is increased by one each time display data is written or read. In the horizontal address increment mode, the horizontal address is increased up to 0x0EF. If more display data is written or read, the vertical address is increased and the horizontal address returns to 0x000.

Vertical address circuit:

The vertical address of the display data RAM is specified by using the vertical address register (R21h) as shown in Figure 5.5.1. The vertical address is increased each by one when one each time display is written or read and horizontal address is increased to last address.

When the vertical address has been increased up to 0x13F and the horizontal address up to the final address, if further display data is read or written, the horizontal and vertical addresses return to 0x000.

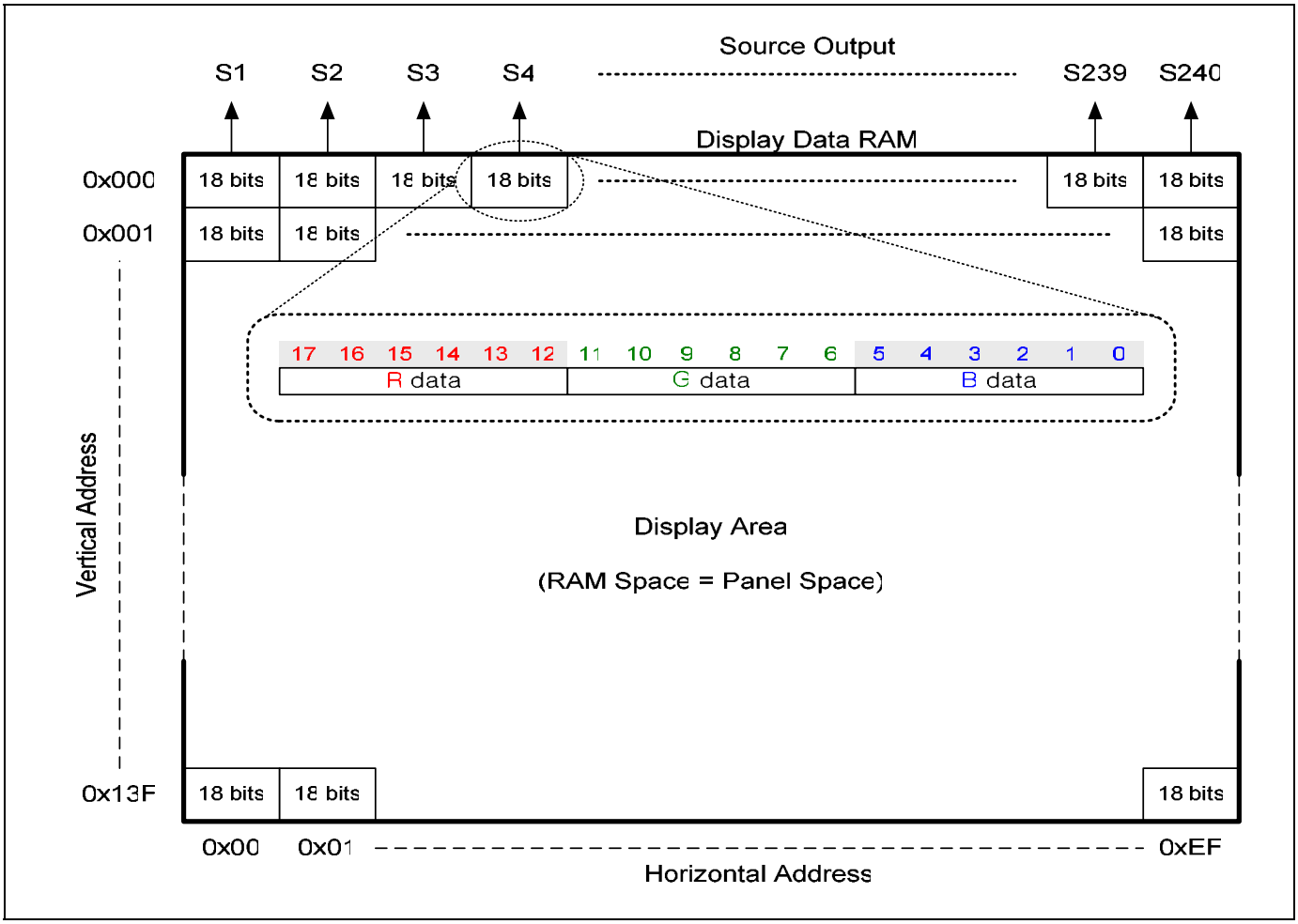


Figure 5.5.1.1 Display Data RAM Construction

5.5.2 DISPLAY DATA ADDRESSING

Address coordinates:

As shown in Figure 1, display data RAM space corresponds to the display area on the panel. The horizontal and vertical addresses make coordinates and their directions make the position of the starting pointing. The direction of the horizontal and vertical addresses is determined by the ID0 and ID1 commands of the control register (R3h).

5.5.3 DISPLAY DATA RAM

Window access mode:

With S6D1121, Any area of the display RAM selected by the MIN horizontal / vertical address registers (R46h and R48h) and MAX horizontal / vertical address registers (R46h and R47h) can be accessed.

First, select the area to be accessed by suing the MIN horizontal / vertical address registers and MAX horizontal / vertical address registers. The address scanning setting is also valid in this mode, in the same manner as when data is normally written to the display RAM. In addition, data can be written from any address by specifying the horizontal address register (R20h) and vertical address register (R21h).

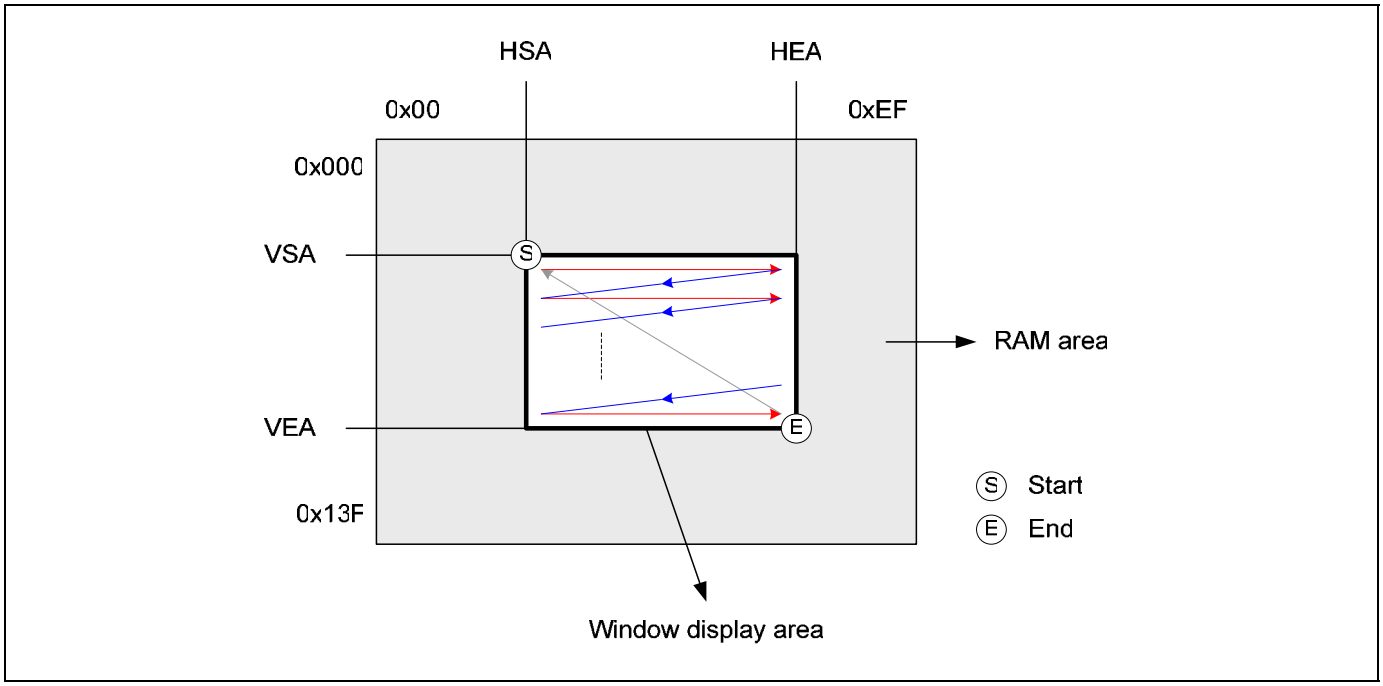


Figure 5.5.3.1 Window Access Mode (AM = 0)

NOTES:
1. When using the window access mode, the relationship between the start point and end point shown in the table below must be established.
2. If invalid address data is set as the MIN/MAX address, operation is not guaranteed.

Item	Address Relationship
Horizontal address	0x00 ≤ MIN Horizontal address (HSA) ≤ MAX Horizontal address (HEA) ≤ 0xEF
Vertical address	0x000 ≤ MIN Vertical address (VSA) ≤ MAX Vertical address (VEA) ≤ 0x13F

5.5.4 DISPLAY DATA RAM WRITE AND READ SEQUENCE

The below figures show the read and write operation with memory.

Read Operation:

In case of 16-/8-bit interface, the LSB of <R><B> color data will not be read. This function is not available in RGB interface mode. Bit assignment RD to DB pins reversely operates against write. On the read operation with TRI command, this operation is not working.

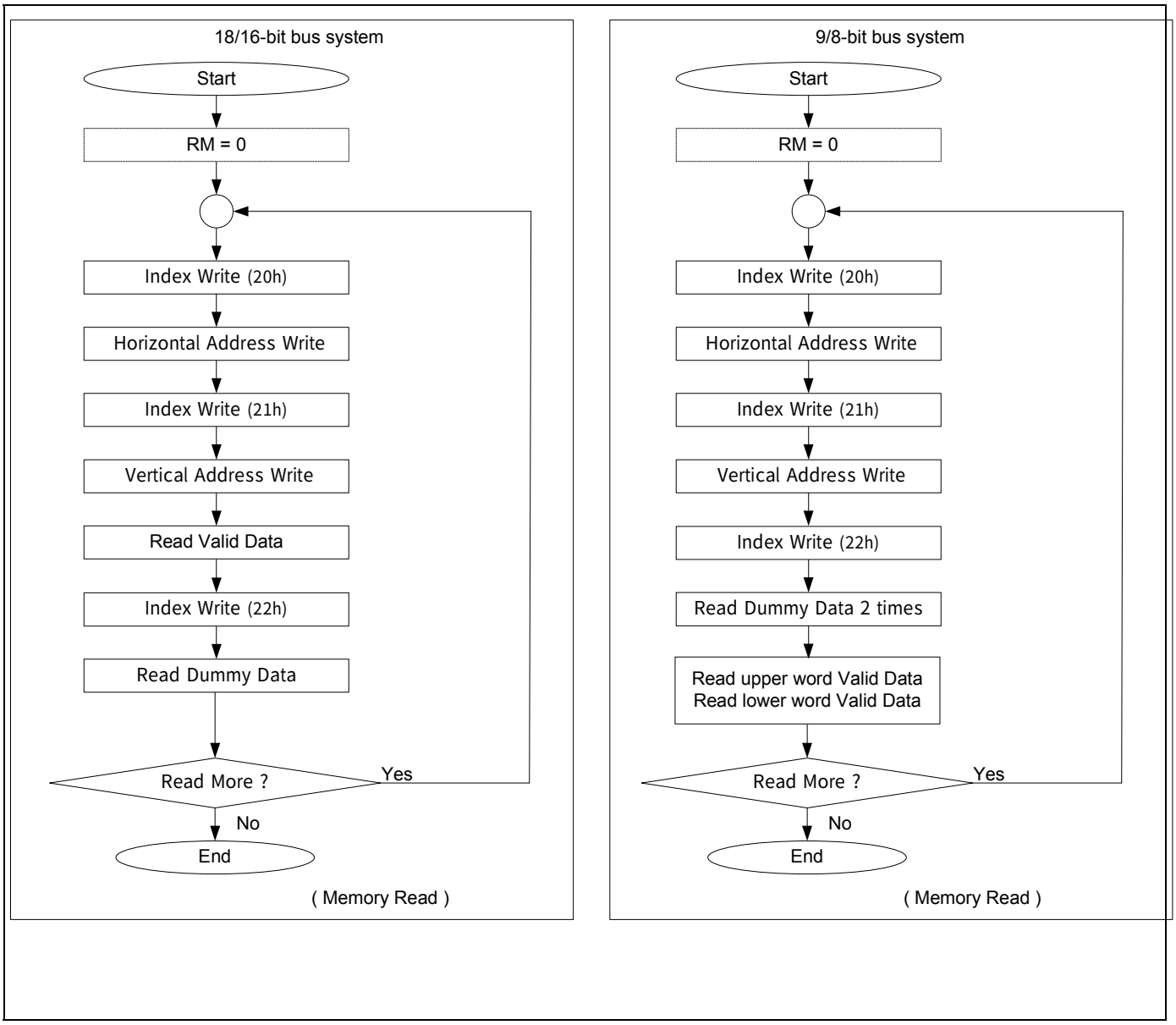


Figure 5.5.4.1 Memory Data Read Sequence

Write Operation:

When the 18-bit RGB interface is in use, 18-bit data is written to RAM via PD17-0. This interface is available on the 262,144-colors. When the 16-bit RGB interface is in use, the MSB is written to its LSB. This interface is available on the 65,536-colors.

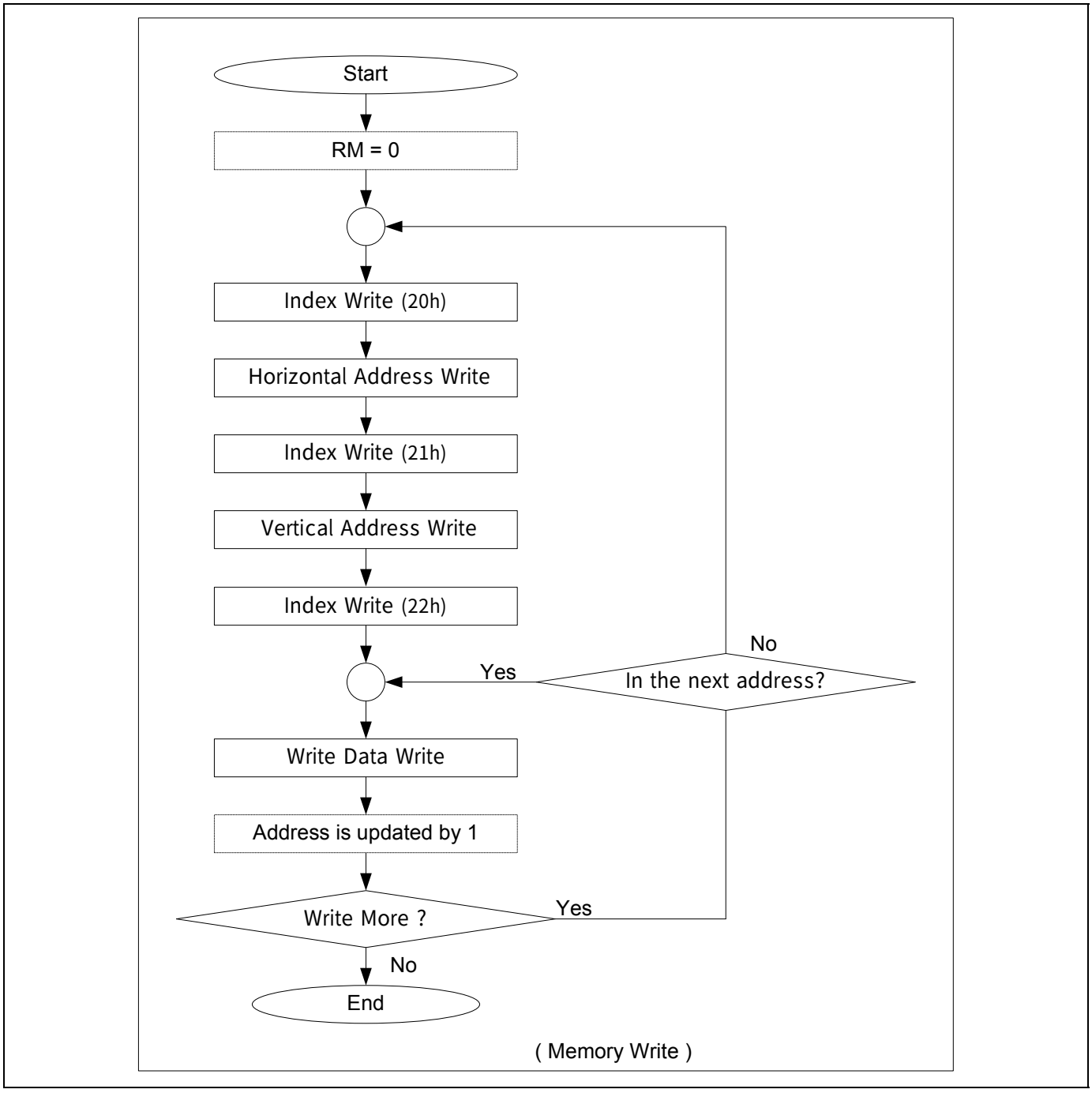


Figure 5.5.4.2 Memory Data Write Sequence

5.5.5 WINDOW DISPLAY SEQUENCE

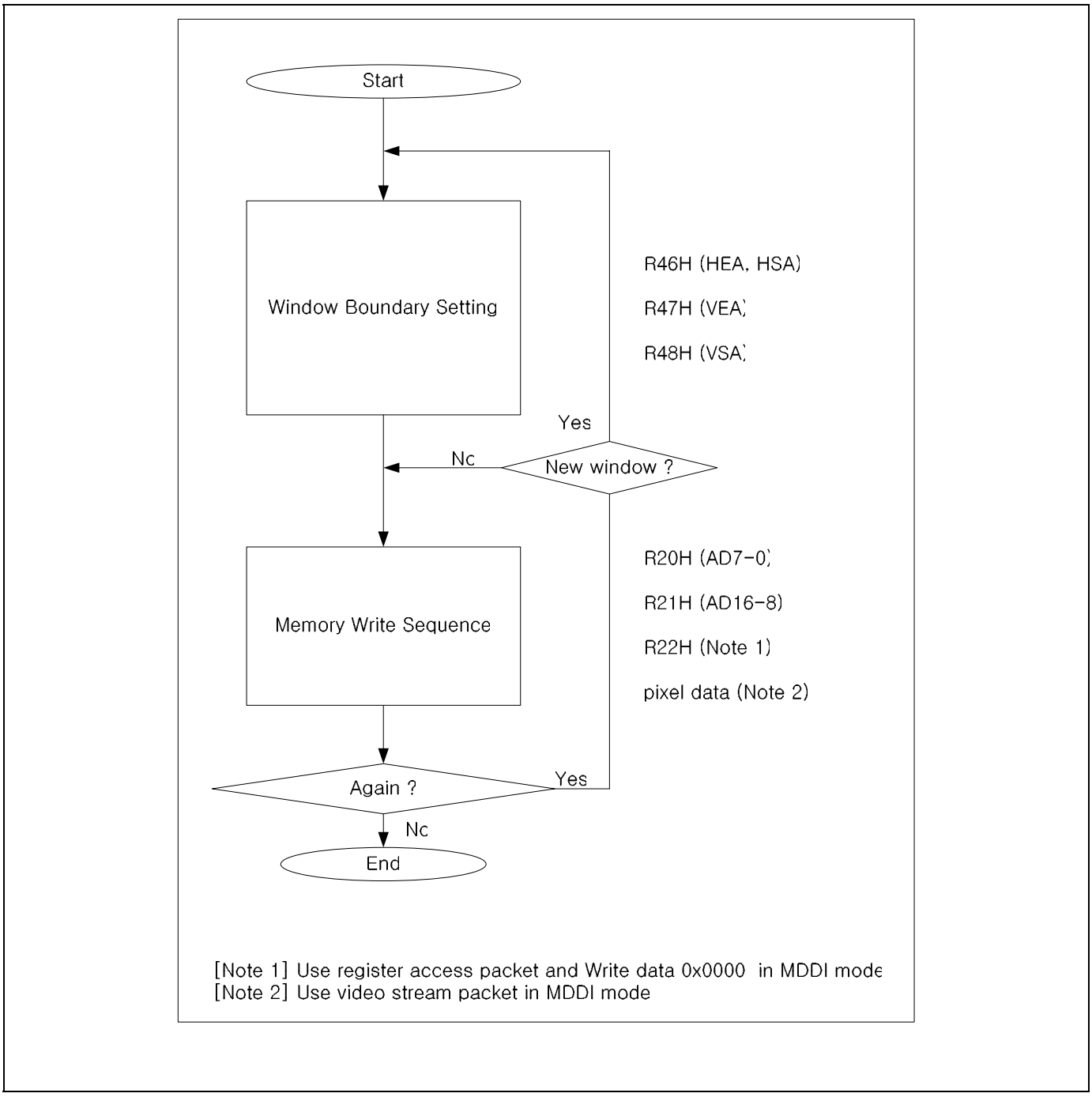


Figure 5.5.5.1 Window Display Sequence

5.6 MTP (MUTI TIME PROGRAMMABLE)

5.6.1 MTP CALIBRATION MODE

S6D1121 supports the MTP function. This figure is a operation diagram of MTP.
Initially, MTP cell is not programmed and has VCOMH (6b'00000). When the external reset is applied, MTP mode is on.

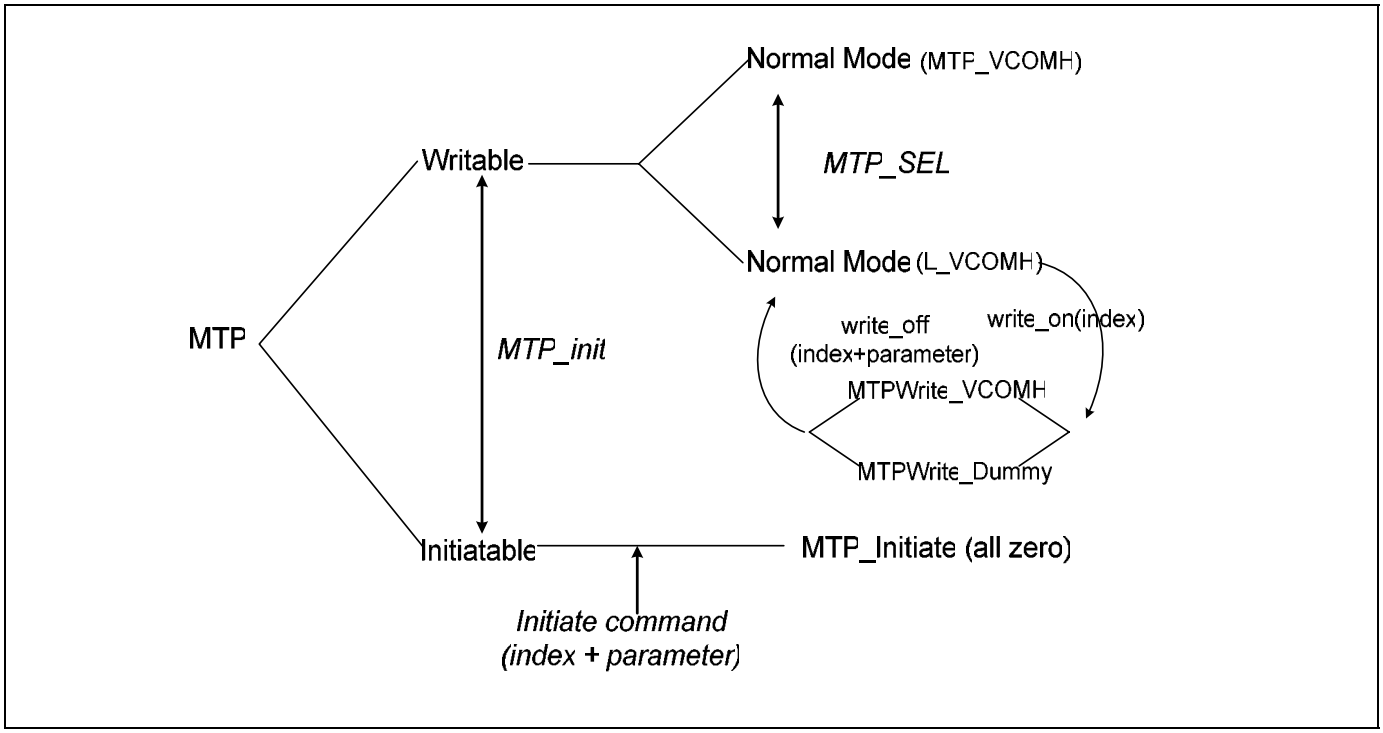


Figure 5.6.1.1 MTP Operation Diagram

5.6.2 MTP CELL STRUCTURE

The MTP has been implemented on the S6D1121. The MTP Cell stores the offset volume for VCOMH calibration after device has been assembled and calibrated on a LCD module. The MTP_EP and MTP_PP pins used for MTP programming.

The MTP block of the S6D1121 consists of one array, which has 7 bits. The MSB of 1 bit is used for protection of MTP mode, and 6 bits are used for VCOMH calibration (VMH0~VMH5) in the direct gate driving method. On the coupling gate driving method, the 6 bits are VMA0 ~ VMA5. MPRT can be read or be written automatically in this LSI.

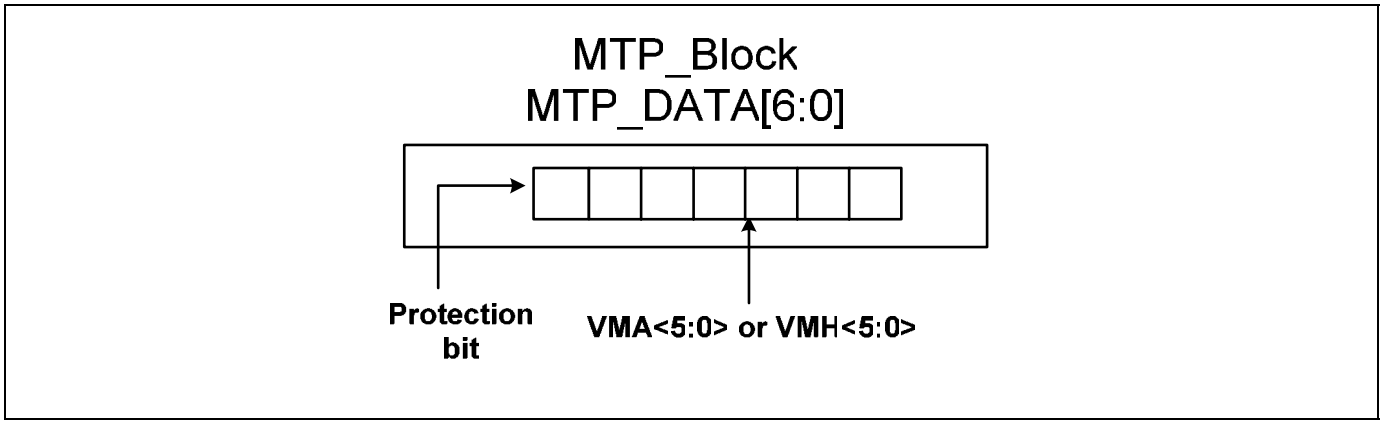


Figure 5.6.2.1 MTP Cell structure

5.6.3 MTP TIMING

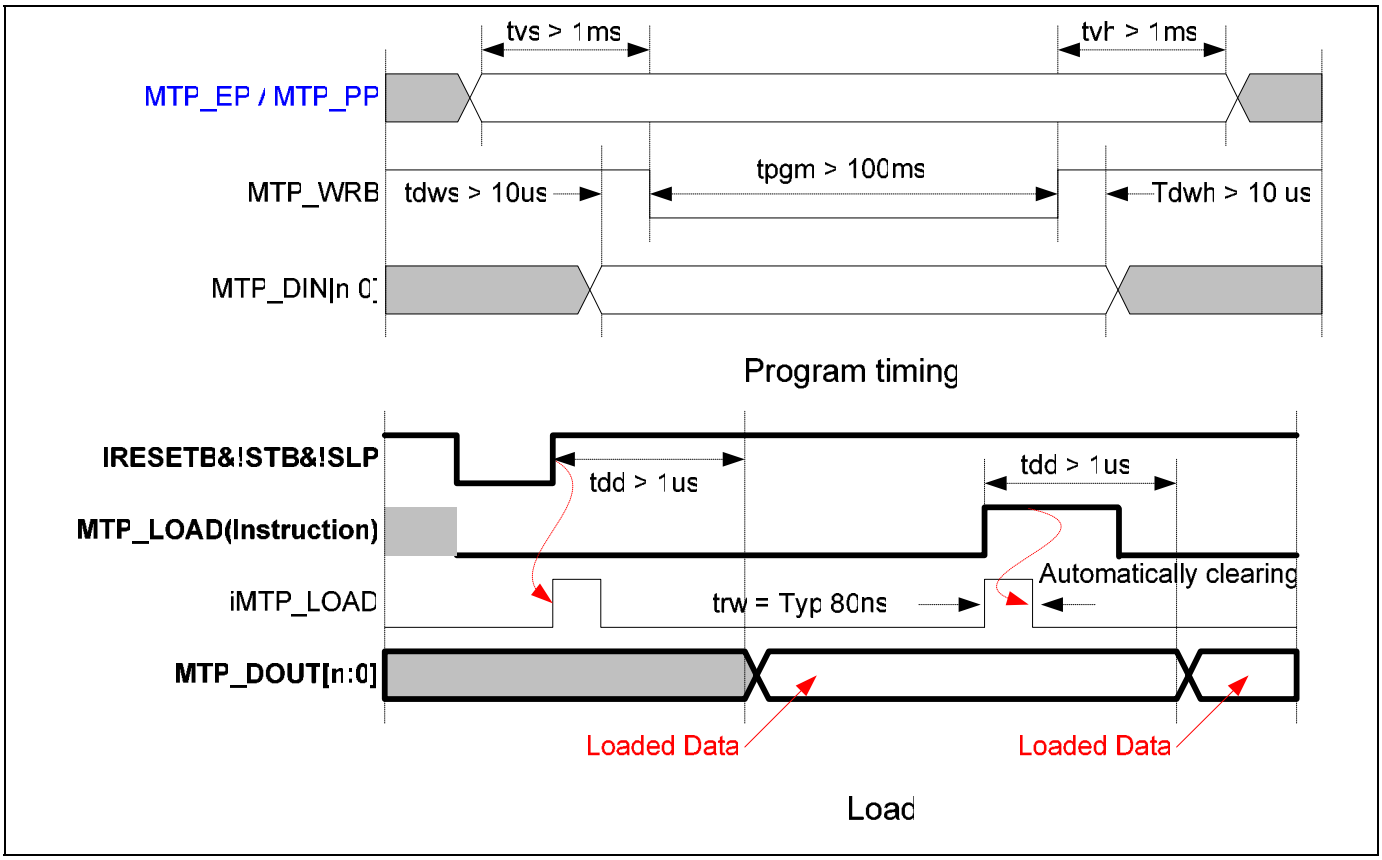


Figure 5.6.3.1 MTP Timing Diagram

5.6.4 MTP SEQUENCE FLOW

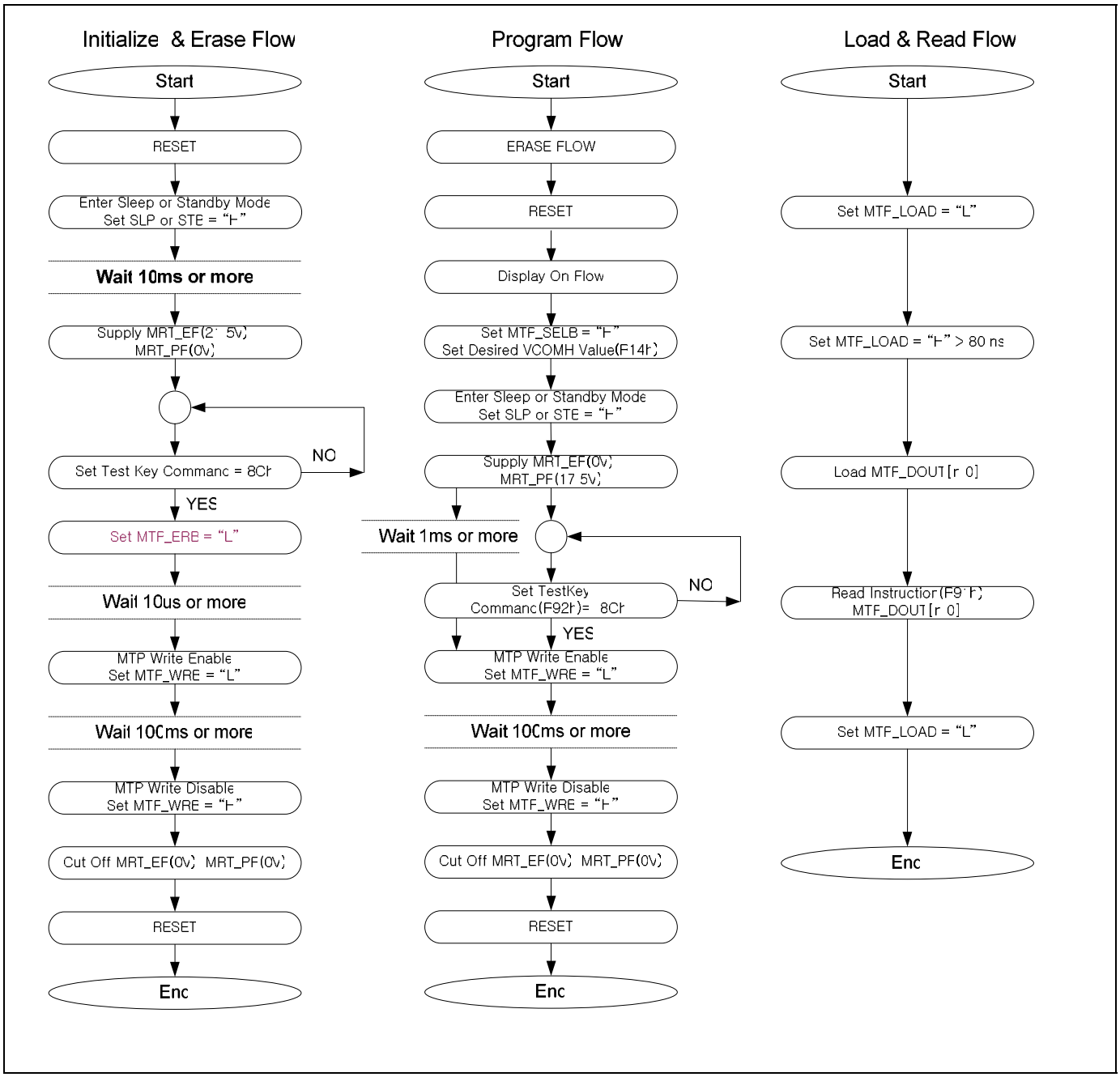


Figure 5.6.4.1 MTP Sequence Flow

NOTE : In MDDI Mode, it doesn't work at STB Mode. So, it is only active at SLP Mode in MDDI

5.7 OSC

S6D1121 can provide R-C oscillation. S6D1121 internal oscillator does not need to be attached to any external resistor. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the oscillator frequency control register setting. Since R-C oscillation stops during the standby mode, power consumption can be reduced.

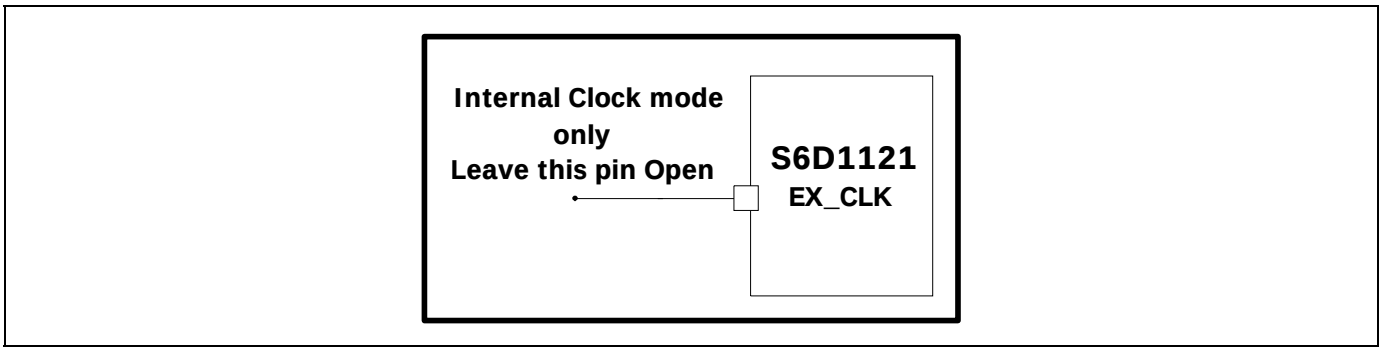


Figure 5.2.12.1 Oscillation Circuit

5.8 POWER SUPPLY SEQUENCE

5.8.1 EXTERNAL POWER ON / OFF SEQUENCE

VDD3 should reach 90% before VCI does so, and vice versa, but in this case, VCI rising time must be faster than VDD3 rising time within 1ms, and VDD3 rising time must be faster than VCI rising time within 1 ms. When regulator cap is 1μF, RESETB must be applied after VCI & VDD3 have been applied. The applied time gap between VCI & VDD3 stable high and RESETB is minimum 1ms. As regulator capacitance becomes larger, this time gap must be increased. Otherwise function is not guaranteed.

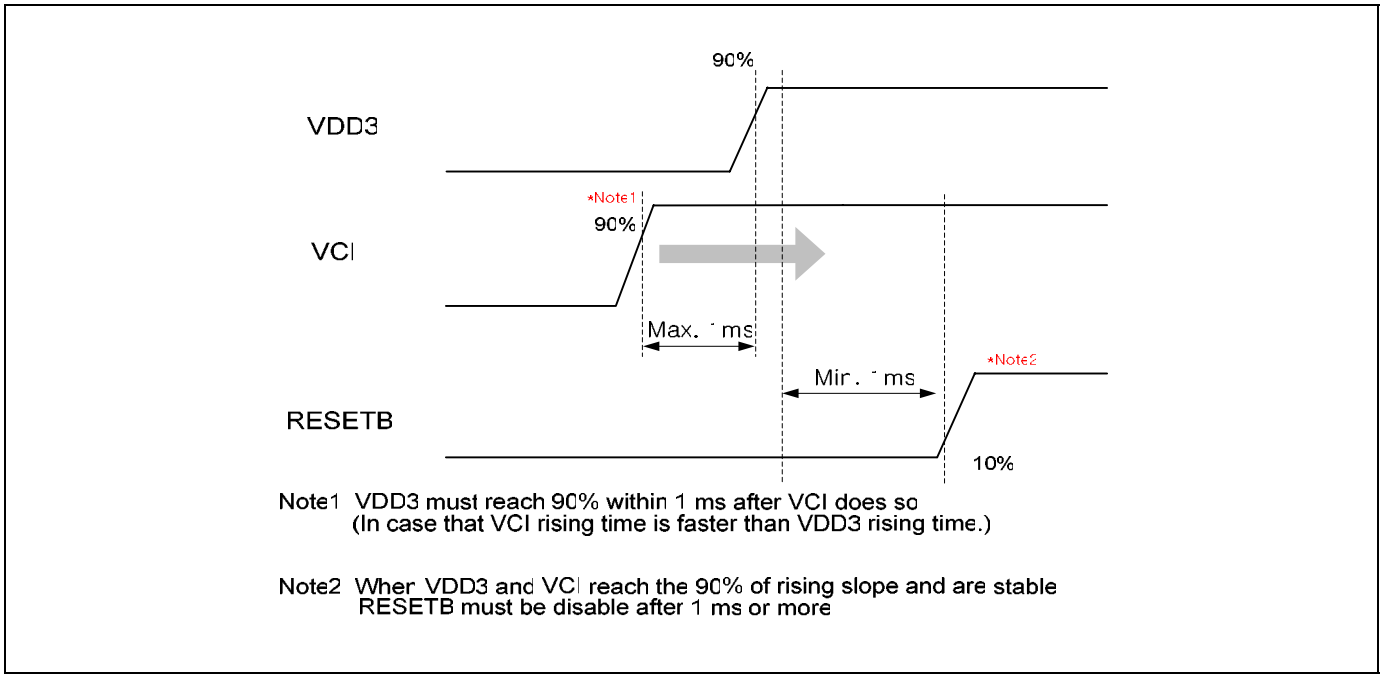


Figure 5.8.1.1 External Power On Sequence

After VCI and VDD3 are stable, normally VCI should fall before VDD3 falls, and VDD3 can fall before VCI falls. VCI falling time must be faster than VDD3 falling time within 1ms, and VDD3 falling time must be faster than VCI falling time within 1 ms.

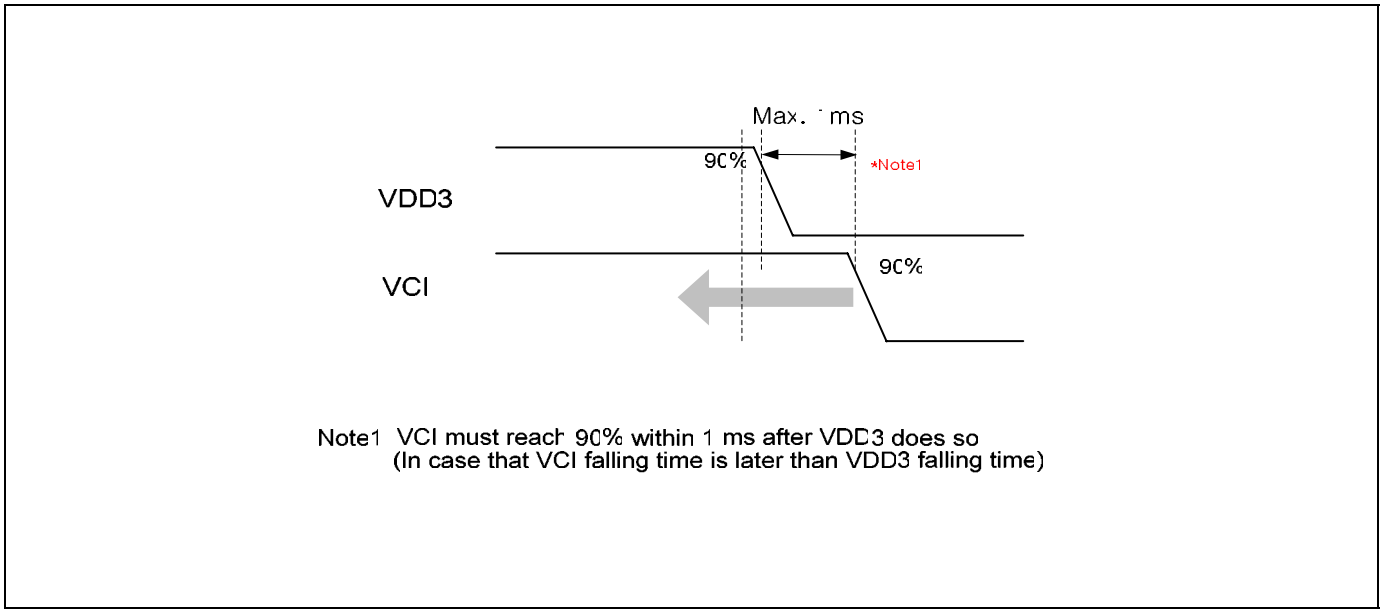


Figure 5.8.1.2 External Power Off Sequence

5.8.2 POWER ON / OFF SEQUENCE OF DIRECT DRIVING MODE WITH VCOM

Apply the power in a sequence as shown in the following figure. The stable time of the oscillation circuit, step-up circuit, and operational amplifier depends on the external resistor or capacitance.

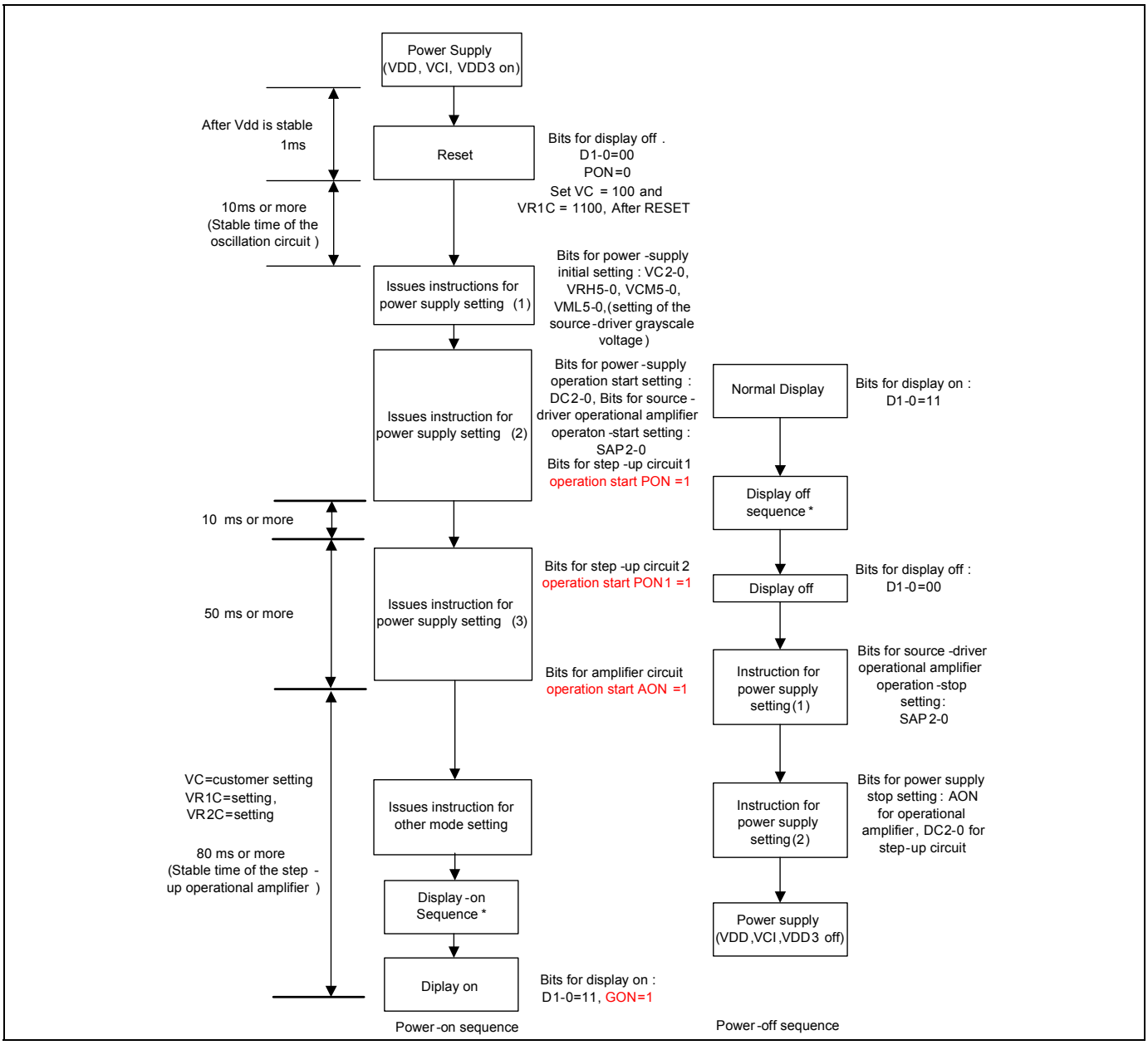


Figure 5.8.2.1 Set up Flow of Direct Driving Mode Power Supply

5.8.3 DIRECT DRIVING MODE INSTRUCTION SETUP FLOW

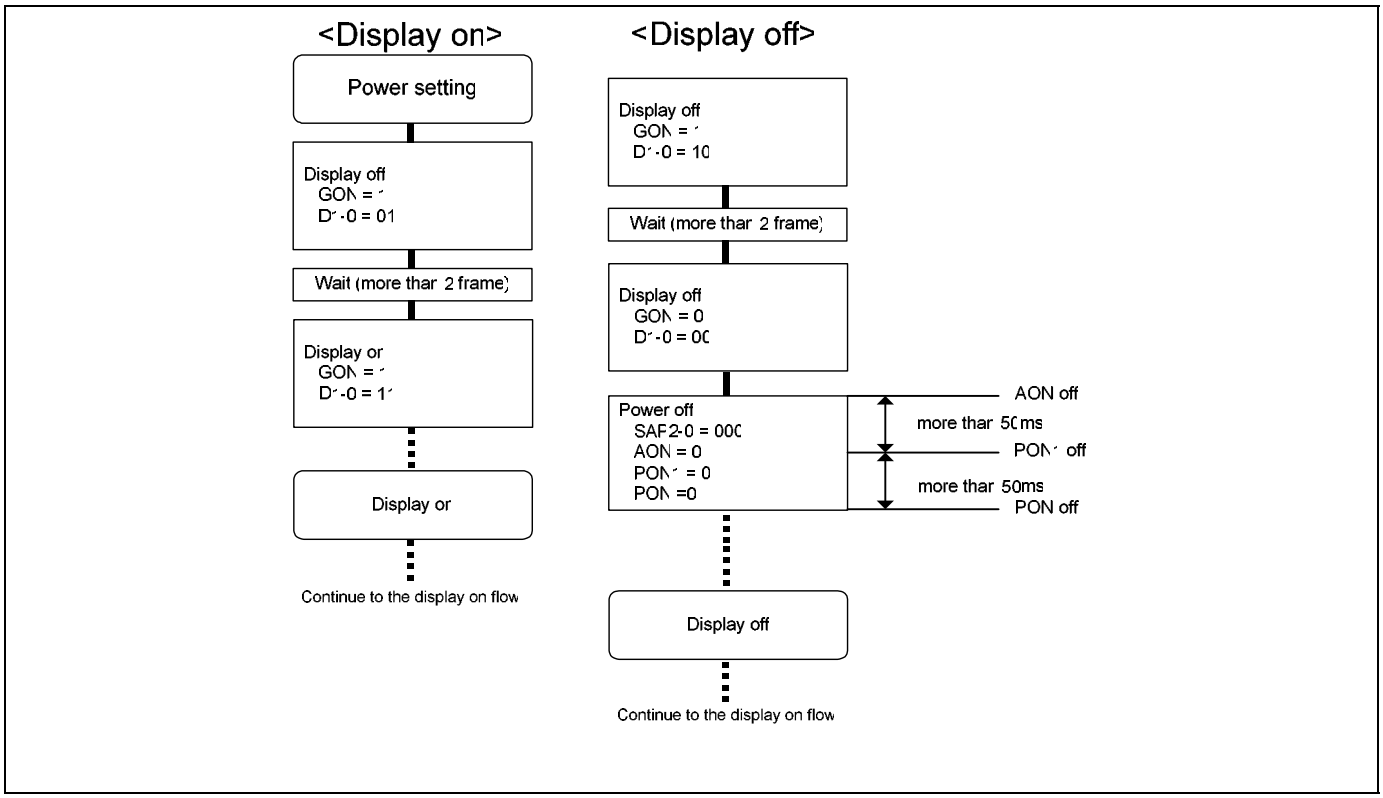


Figure 5.8.3.1 Direct driving mode instruction set up flow

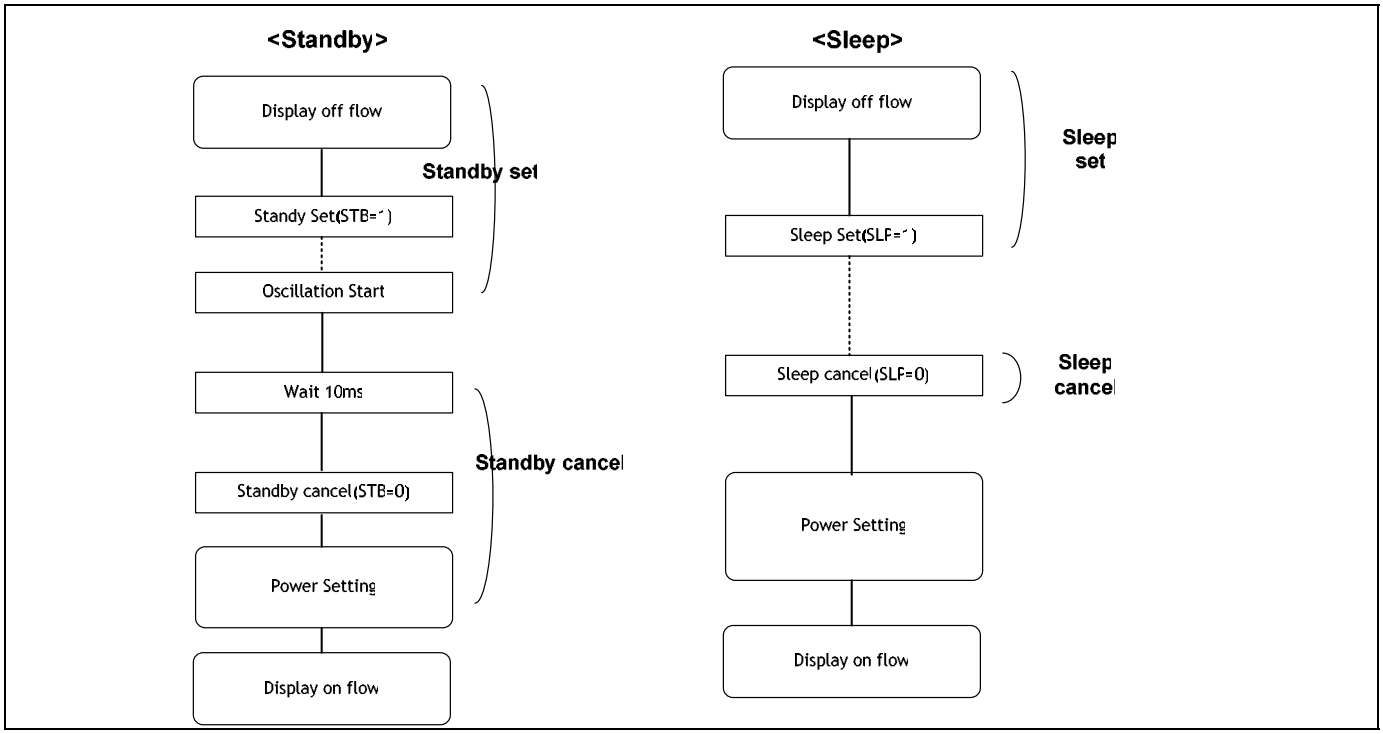


Figure 5.8.3.2 Direct driving mode instruction setup flow (continued)

5.8.4 POWER ON / OFF SEQUENCE OF COUPLING DRIVING MODE WITH VCOM

Apply the power in a sequence as shown in the following figure. The stable time of the oscillation circuit, step-up circuit, and operational amplifier depends on the external resistor or capacitance.

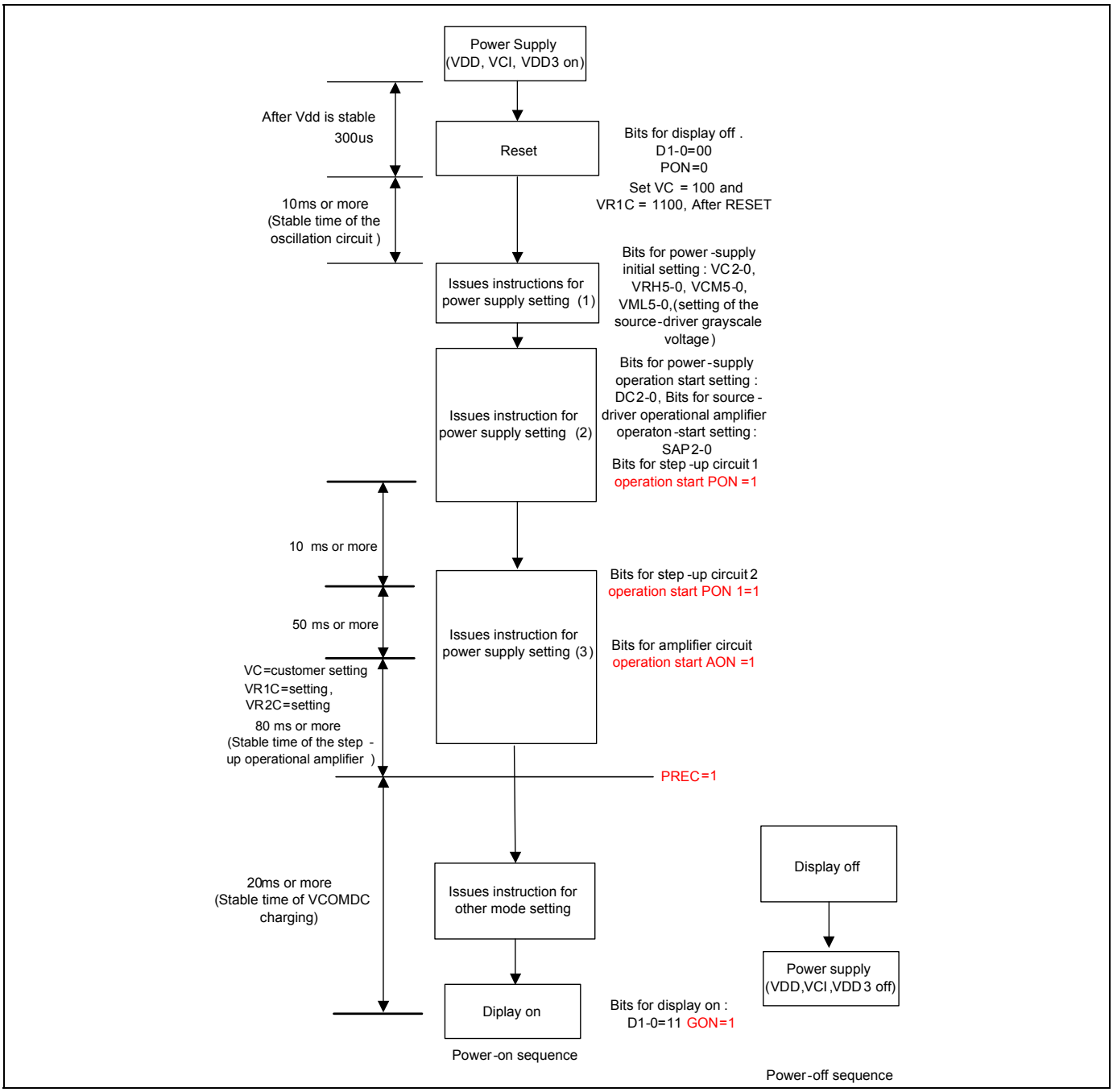


Figure 5.8.4.1 Set up Flow of Coupling Driving Mode Power Supply

5.8.5 COUPLING DRIVING MODE INSTRUCTION SETUP FLOW

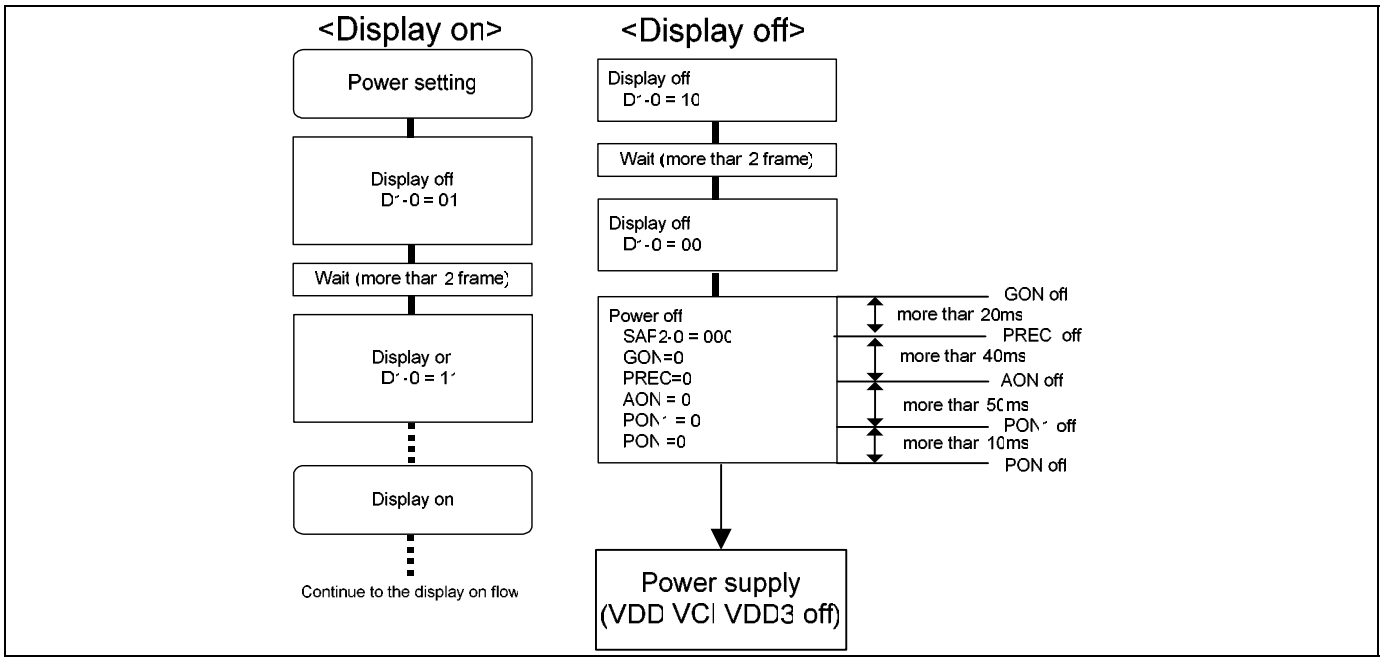


Figure 5.8.5.1 Coupling driving mode instruction set up flow

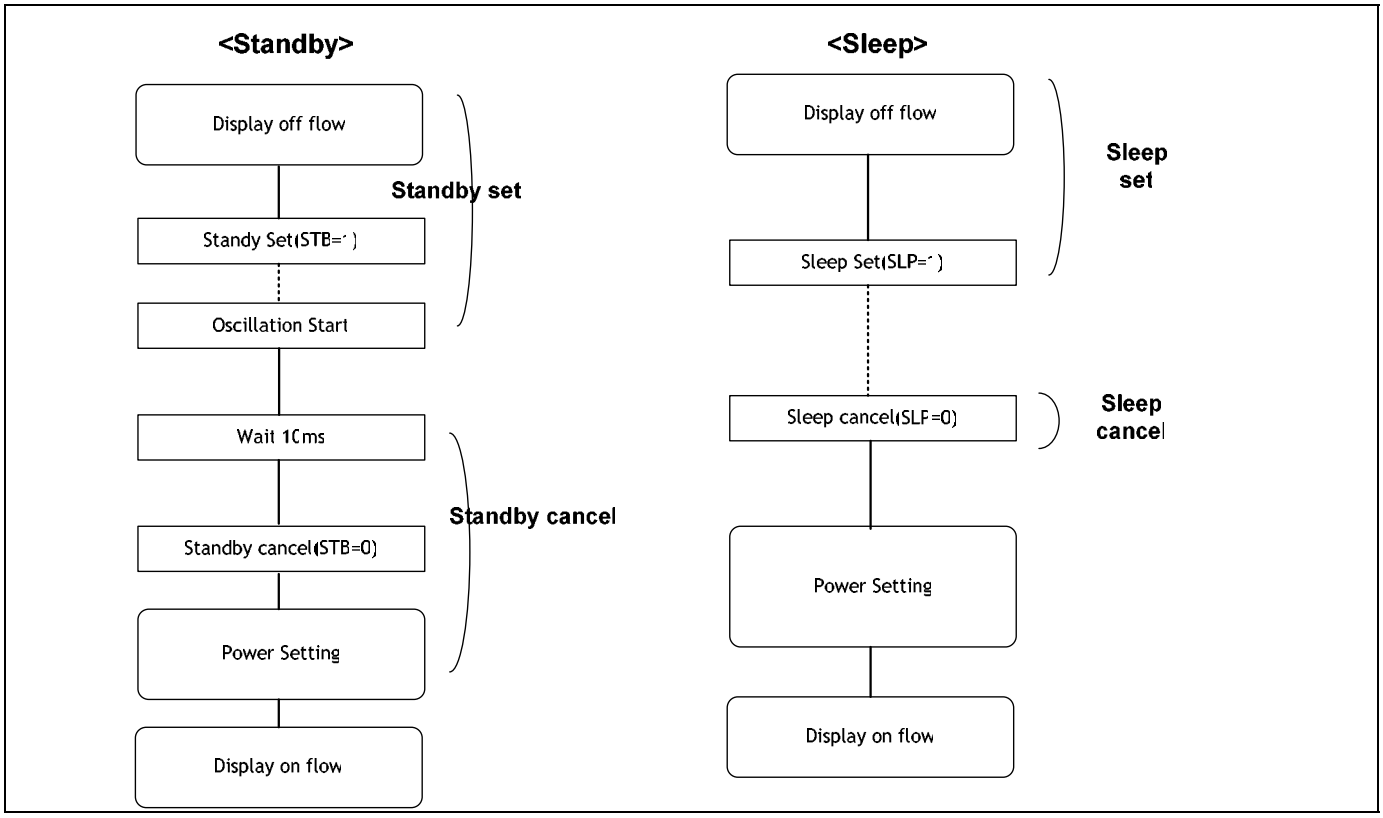


Figure 5.8.5.2 Coupling driving mode instruction setup flow (continued)

5.9 POWER CIRCUIT

5.9.1 POWER CIRCUIT ARCHITECTURE

The following figure shows a configuration of the voltage generation circuit for S6D1121. The step-up circuits consist of step-up circuits 1 to 2. Step-up circuit1 doubles and triple the voltage supplied to VCI1 for AVDD level. Step-up circuit2 makes 7.5 ~ 16.0V for VGH level (=AVDD + VR1 + VR2), and make –(AVDD+VR1) level for VGL level. VGL is VGLROUT regulator power voltage. VR1 block makes 2.0 ~ 5.0V for VGL. VR2 block makes 2.0 ~ 5.0V for VGH level. These step-up circuits generate power supplies AVDD, GVDD, VGH, VGL, VGLROUT, VR1, VR2 and VCOM. Reference voltages GVDD, VCOM, and VGLROUT for the grayscale voltage are amplified from the voltage adjustment circuit. Connect VCOM to the TFT panel.

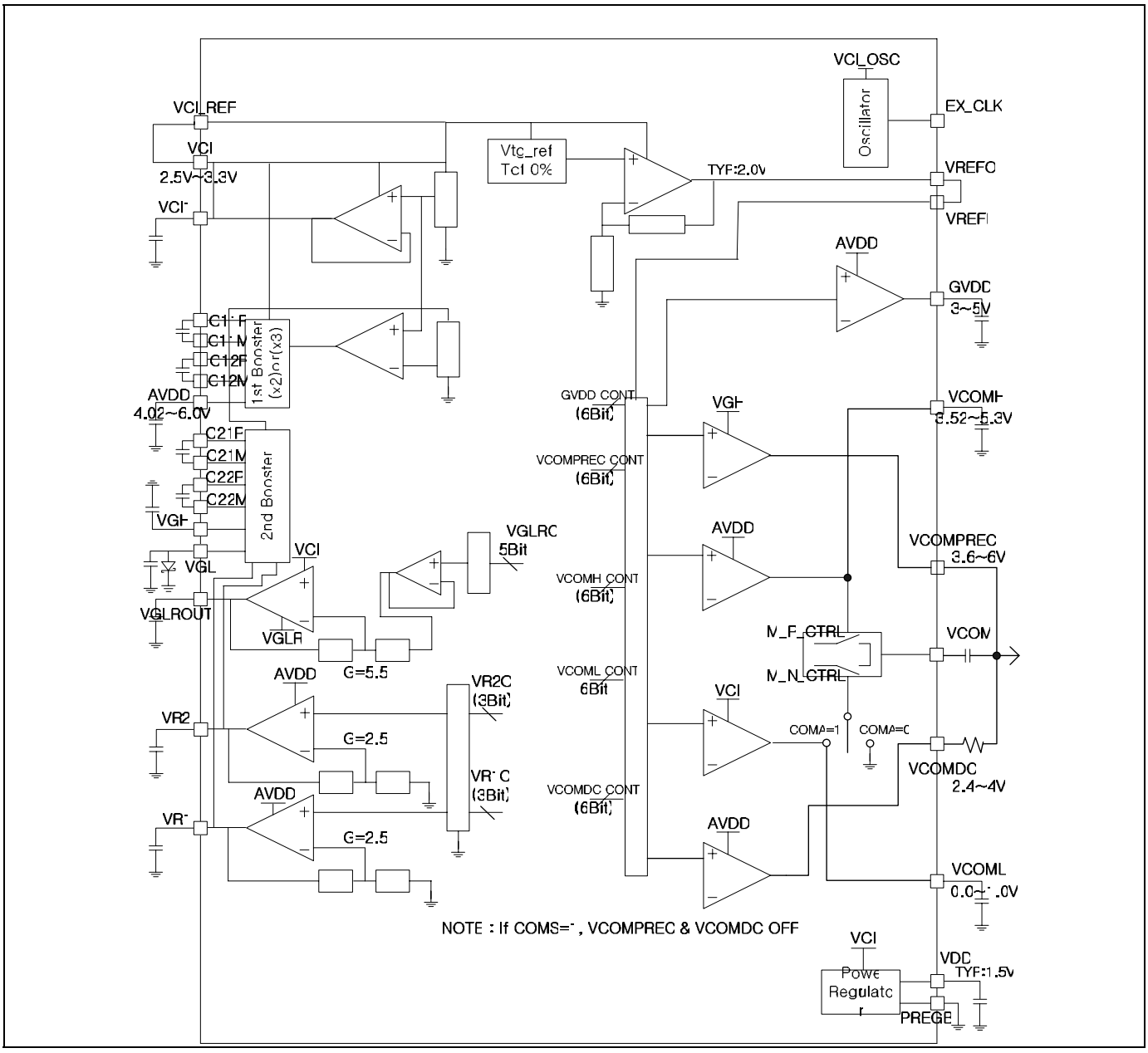


Figure 5.9.1.1 Configuration of the Internal Power-Supply Circuit

NOTE:
Use the 1uF capacitor.

5.9.2 PATTERN DIAGRAMS FOR VOLTAGE SETTING

The following figure shows a pattern diagram for the voltage setting and an example of waveforms.

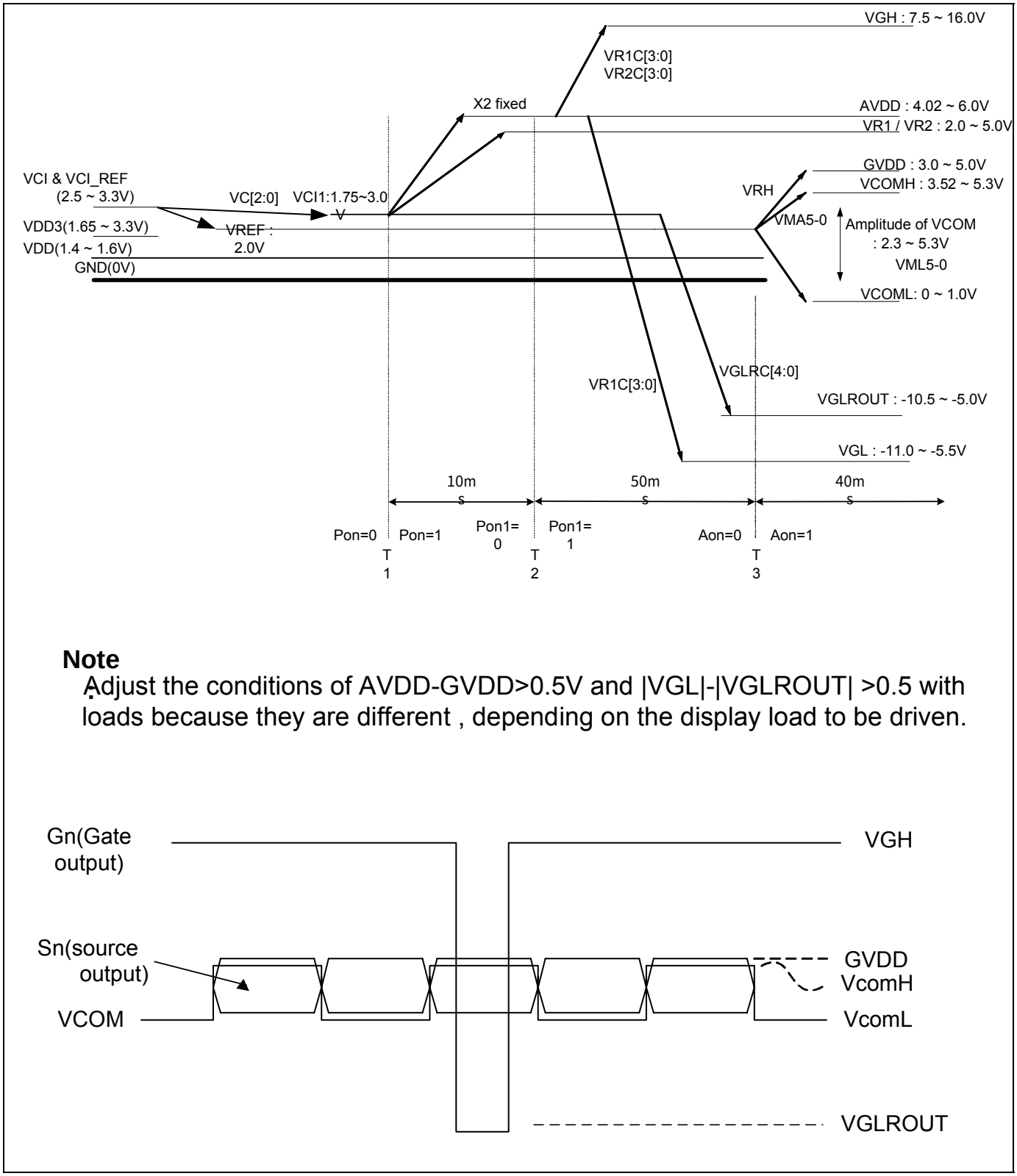


Figure 5.9.2.1 Pattern Diagram and An Example of Waveforms

5.10 GAMMA CURVE CORRECTION

5.10.1 GAMMA ADJUSTMENT FUNCTION

The S6D1121 provides the gamma adjustment function to display 262,144 colors simultaneously. The gamma adjustment executed by the micro adjustment register and the amplitude adjustment register determines 14 grayscale levels. Furthermore, since the micro-adjustment register and amplitude-adjustment register have the positive polarities and negative polarities, adjust them to match LCD panel respectively.

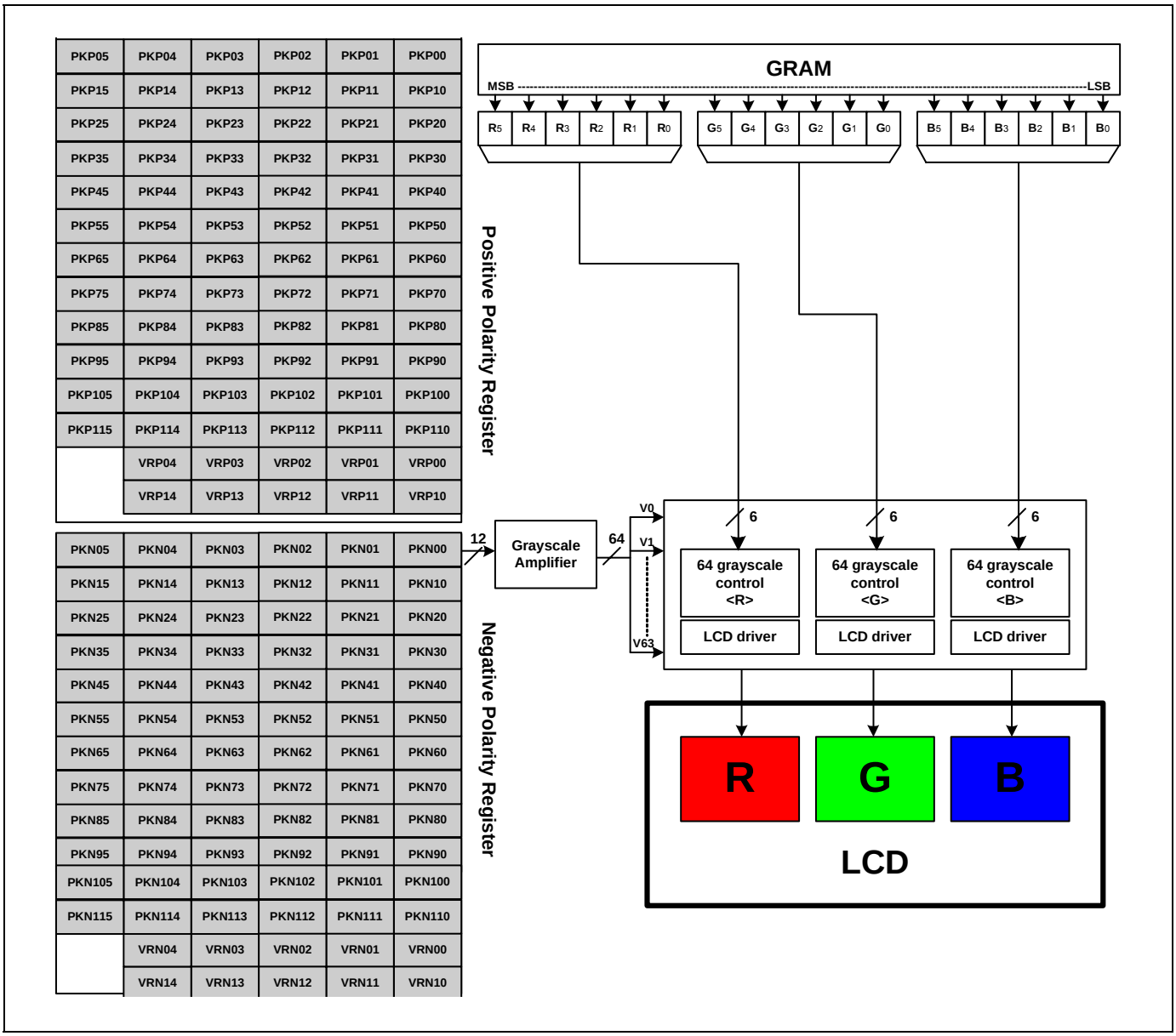


Figure 5.10.1.1 Grayscale control

5.10.2 STRUCTURE OF GRAYSCALE AMPILIFIER

The structure of the grayscale amplifier is shown as below. Determine 8-level (VIN0-VIN11) by the amplitude adjuster and the micro adjustment register. The internal ladder resistance splits each level and levels from V0 to V63 are generated.

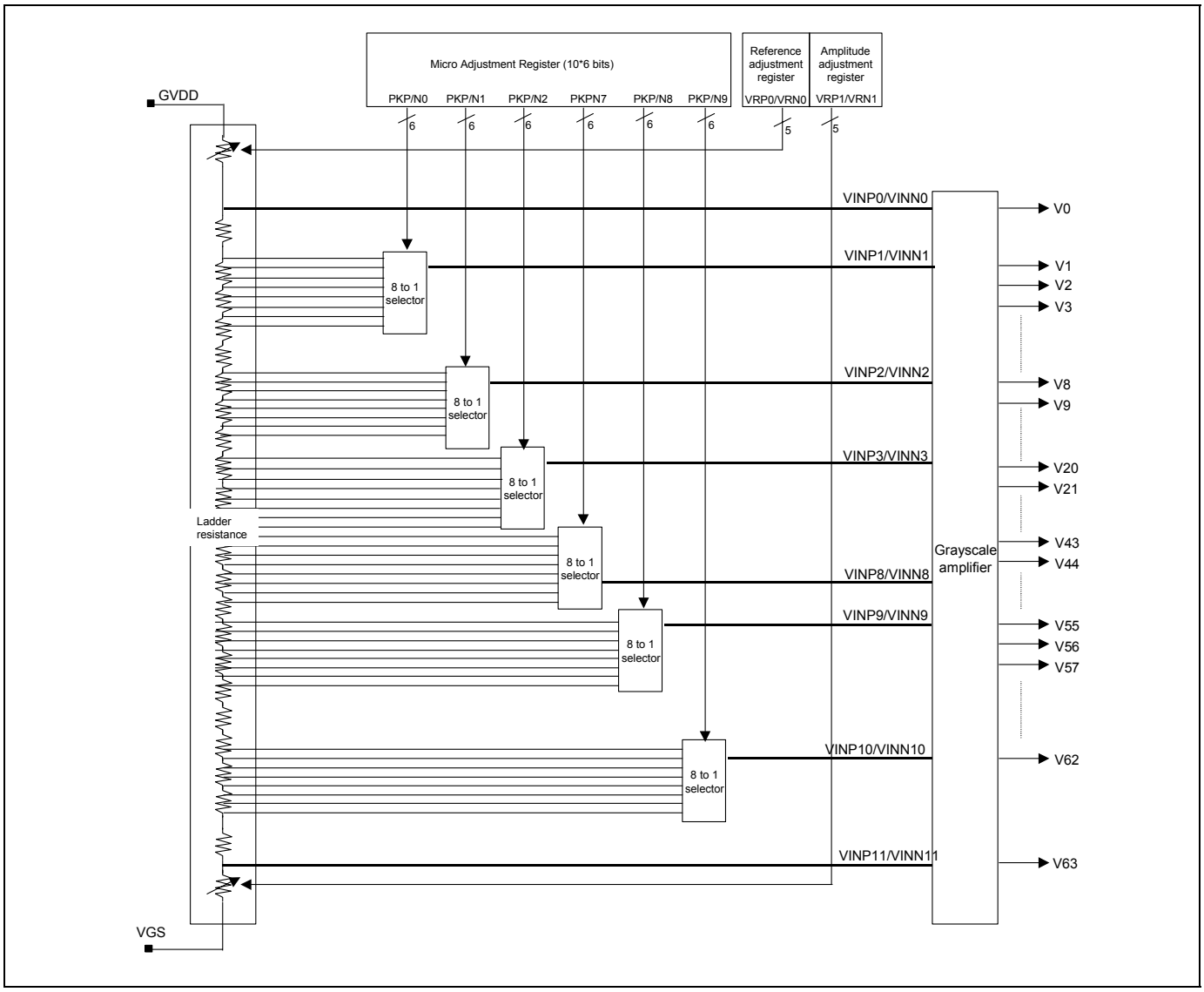


Figure 5.10.2.1 Structure of grayscale amplifier

5.10.3 GAMMA ADJUSTMENT REGISTER

This block has the registers to set up the grayscale voltage according to the gamma specification of the LCD panel. These registers can be independently set up to positive/negative polarities and there are 3 types of register groups to adjust gradient and amplitude on number of the grayscale, characteristics of the grayscale voltage. (Average <R><G><B> are common.) The following figure indicates the operation of each adjusting register.

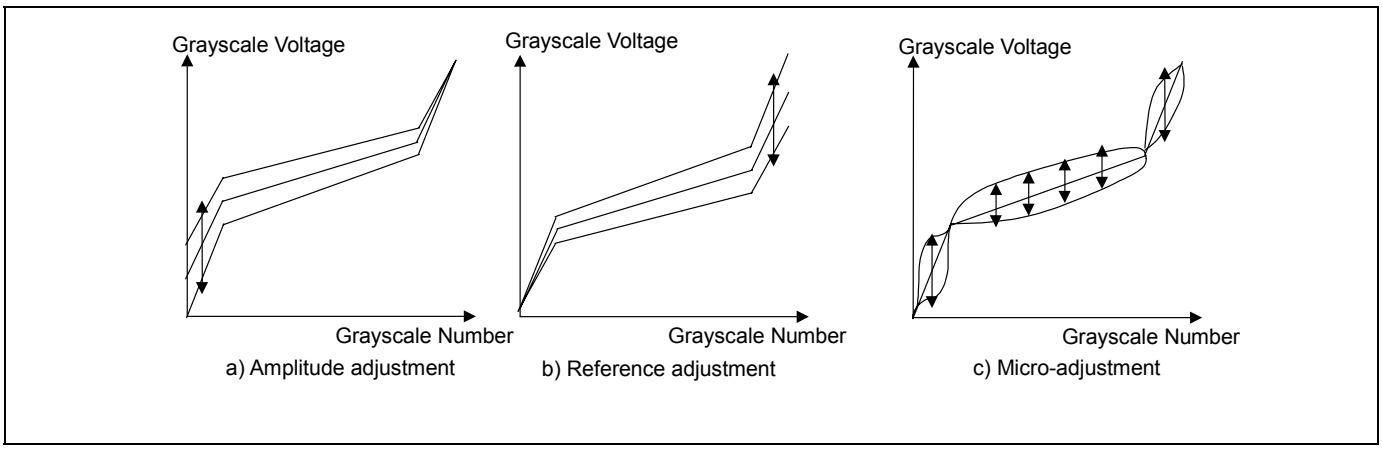


Figure 5.10.3 Operation of Adjusting Register

a) Amplitude adjustment resistor

The amplitude-adjusting resistor is used to adjust the amplitude of the grayscale voltage. To accomplish the adjustment, it controls the variable resistor (VRP (N)) of the ladder resistor for the grayscale voltage generator located at lower side of the ladder resistor. (Adjust upper side by input GVDD level.) Also, there is an independent resistor on the positive/negative polarities as well as the gradient-adjusting resistor.

b) Reference adjustment resistor

The Reference-adjusting resistor is used to adjust the reference of the grayscale voltage. To accomplish the adjustment, it controls the variable resistor (VRP(N)0) of the ladder resistor for the grayscale voltage generator located at upper side of the ladder resistor.

c) Micro adjustment resistor

The micro adjustment resistor is used to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls each reference voltage level by the 64 to 1 selector towards the 64-leveled reference voltage generated from the ladder resistor. There is also an independent resistor on the positive/negative polarities as well as other adjusting resistors.

Table 5.10.3 Gamma correction registers

Register	Positive polarity	Negative polarity	Set-up contents
Reference adjustment	VRP0[4:0]	VRN0[4:0]	Variable resistor VRP(N)0 –sets grayscale 0
Micro-adjustment	PKP0[5:0]	PKN0[5:0]	The voltage of grayscale number 1 is selected by the 8 to 1 selector
	PKP1[5:0]	PKN1[5:0]	The voltage of grayscale number 5 is selected by the 8 to 1 selector
	PKP2[5:0]	PKN2[5:0]	The voltage of grayscale number 6 is selected by the 8 to 1 selector
	PKP3[5:0]	PKN3[5:0]	The voltage of grayscale number 8 is selected by the 8 to 1 selector
	PKP4[5:0]	PKN4[5:0]	The voltage of grayscale number 16 is selected by the 8 to 1 selector
	PKP5[5:0]	PKN5[5:0]	The voltage of grayscale number 23 is selected by the 8 to 1 selector
	PKP6[5:0]	PKN6[5:0]	The voltage of grayscale number 40 is selected by the 8 to 1 selector
	PKP7[5:0]	PKN7[5:0]	The voltage of grayscale number 47 is selected by the 8 to 1 selector
	PKP8[5:0]	PKN8[5:0]	The voltage of grayscale number 55 is selected by the 8 to 1 selector
	PKP9[5:0]	PKN9[5:0]	The voltage of grayscale number 57 is selected by the 8 to 1 selector
	PKP10[5:0]	PKN10[5:0]	The voltage of grayscale number 58 is selected by the 8 to 1 selector
	PKP11[5:0]	PKN11[5:0]	The voltage of grayscale number 62 is selected by the 8 to 1 selector
Amplitude adjustment	VRP1[4:0]	VRN1[4:0]	Variable resistor VRP(N)1 –sets grayscale 63

5.10.4 LADDER RESISTOR/8 TO 1 SELECTOR

This block outputs the reference voltage of the grayscale voltage. There are two ladder resistors including the variable resistor and the 8 to 1 selector which selects the voltage generated by the ladder resistance voltage. The variable resistors and 8 to 1 resistors are controlled by the gamma resistor. Also, there are pins that connect to the external volume resistor. In addition, it allows compensating the dispersion of length from one panel to another.

5.10.4.1 VARIABLE RESISTOR

Variable resistors are used for the gradient for the amplitude adjustment and reference adjustment (VRP (N)). The resistance value is set by the gradient adjusting resistor and the amplitude adjustment resistor as shown below.

Table 5.10.4.1.1 Reference Adjustment

Register value VRP(N)0[4:0]	Resistance value VRP(N)0
00000	0R
00001	1R
00010	2R
. . .	. . .
11101	29R
11110	30R
11111	31R

Table 5.10.4.1.2 Amplitude Adjustment

Register value VRP(N)1[4:0]	Resistance value VRP(N)1
00000	0R
00001	1R
00010	2R
. . .	. . .
11101	29R
11110	30R
11111	31R

5.10.4.2 THE 64 TO 1 SELECTOR

In the 64 to 1 selector, the voltage level must be selected given by the ladder resistance and the micro-adjusting register. The output voltage is given by the six types of the reference voltage, the VIN1 to VIN12.

Following figure explains the relationship between the micro-adjusting register and the selected voltage.

Table 5.10.4.2.1 Relationship Table between Micro-adjustment Register and Selected Voltage

Register PKP(N) [5:0]	VINP(N) 1	VINP(N) 2	VINP(N) 3	VINP(N) 4	VINP(N) 5	VINP(N) 6	VINP(N) 7	VINP(N) 8	VINP(N) 9	VINP(N) 10	VINP(N) 11	VINP(N) 12
000000	1	9	9	23	34	46	66	73	80	88	88	96
000001	2	10	10	24	35	47	67	74	81	89	89	97
000010	3	11	11	25	36	48	68	75	82	90	90	98
000011	4	12	12	26	37	49	69	76	83	91	91	99
000100	5	13	13	27	38	50	70	77	84	92	92	100
000101	6	14	14	28	39	51	71	78	85	93	93	101
000110	7	15	15	29	40	52	72	79	86	94	94	102
000111	8	16	16	30	41	53	73	80	87	95	95	103
001000	9	17	17	31	42	54	74	81	88	96	96	104
001001	10	18	18	32	43	55	75	82	89	97	97	105
001010	11	19	19	33	44	56	76	83	90	98	98	106
001011	12	20	20	34	45	57	77	84	91	99	99	107
001100	13	21	21	35	46	58	78	85	92	100	100	108
001101	14	22	22	36	47	59	79	86	93	101	101	109
001110	15	23	23	37	48	60	80	87	94	102	102	110
001111	16	24	24	38	49	61	81	88	95	103	103	111
010000	17	25	25	39	50	62	82	89	96	104	104	112
010001	18	26	26	40	51	63	83	90	97	105	105	113
010010	19	27	27	41	52	64	84	91	98	106	106	114
010011	20	28	28	42	53	65	85	92	99	107	107	115
010100	21	29	29	43	54	66	86	93	100	108	108	116
010101	22	30	30	44	55	67	87	94	101	109	109	117
010110	23	31	31	45	56	68	88	95	102	110	110	118
010111	24	32	32	46	57	69	89	96	103	111	111	119
011000	25	33	33	47	58	70	90	97	104	112	112	120
011001	26	34	34	48	59	71	91	98	105	113	113	121
011010	27	35	35	49	60	72	92	99	106	114	114	122
011011	28	36	36	50	61	73	93	100	107	115	115	123
011100	29	37	37	51	62	74	94	101	108	116	116	124
011101	30	38	38	52	63	75	95	102	109	117	117	125
011110	31	39	39	53	64	76	96	103	110	118	118	126
011111	32	40	40	54	65	77	97	104	111	119	119	127
100000	33	41	41	55	66	78	98	105	112	120	120	128
100001	34	42	42	56	67	79	99	106	113	121	121	129
100010	35	43	43	57	68	80	100	107	114	122	122	130
100011	36	44	44	58	69	81	101	108	115	123	123	131
100100	37	45	45	59	70	82	102	109	116	124	124	132
100101	38	46	46	60	71	83	103	110	117	125	125	133
100110	39	47	47	61	72	84	104	111	118	126	126	134
100111	40	48	48	62	73	85	105	112	119	127	127	135
101000	41	49	49	63	74	86	106	113	120	128	128	136
101001	42	50	50	64	75	87	107	114	121	129	129	137

101010	43	51	51	65	76	88	108	115	122	130	130	138
101011	44	52	52	66	77	89	109	116	123	131	131	139
101100	45	53	53	67	78	90	110	117	124	132	132	140
101101	46	54	54	68	79	91	111	118	125	133	133	141
101110	47	55	55	69	80	92	112	119	126	134	134	142
101111	48	56	56	70	81	93	113	120	127	135	135	143
110000	49	57	57	71	82	94	114	121	128	136	136	144
110001	50	58	58	72	83	95	115	122	129	137	137	145
110010	51	59	59	73	84	96	116	123	130	138	138	146
110011	52	60	60	74	85	97	117	124	131	139	139	147
110100	53	61	61	75	86	98	118	125	132	140	140	148
110101	54	62	62	76	87	99	119	126	133	141	141	149
110110	55	63	63	77	88	100	120	127	134	142	142	150
110111	56	64	64	78	89	101	121	128	135	143	143	151
111000	57	65	65	79	90	102	122	129	136	144	144	152
111001	58	66	66	80	91	103	123	130	137	145	145	153
111010	59	67	67	81	92	104	124	131	138	146	146	154
111011	60	68	68	82	93	105	125	132	139	147	147	155
111100	61	69	69	83	94	106	126	133	140	148	148	156
111101	62	70	70	84	95	107	127	134	141	149	149	157
111110	63	71	71	85	96	108	128	135	142	150	150	158
111111	64	72	72	86	97	109	129	136	143	151	151	159

Table 5.10.4.2.2 Gamma Adjusting Voltage Formula (Positive polarity)

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINN0	V32	V40+(V23-V40)*8/17.1
V1	VINN1	V33	V40+(V23-V40)*7/17.1
V2	V5+(V1-V5)*(9/13)	V34	V40+(V23-V40)*6/17.1
V3	V5+(V1-V5)*(6/13)	V35	V40+(V23-V40)*5/17.1
V4	V5+(V1-V5)*(2.5/13))	V36	V40+(V23-V40)*4/17.1
V5	VINN2	V37	V40+(V23-V40)*3/17.1
V6	VINN3	V38	V40+(V23-V40)*217.1
V7	V8+(V6-V8)*1/2	V39	V40+(V23-V40)*1/17.1
V8	VINN4	V40	VINN7
V9	V16+(V8-V16)*7.6/8.9	V41	V47+(V40-V47)*6.4/7.4
V10	V16+(V8-V16)*6.3/8.9	V42	V47+(V40-V47)*5.4/7.4
V11	V16+(V8-V16)*5/8.9	V43	V47+(V40-V47)*4.4/7.4
V12	V16+(V8-V16)*4/8.9	V44	V47+(V40-V47)*3.4/7.4
V13	V16+(V8-V16)*3/8.9	V45	V47+(V40-V47)*2.4/7.4
V14	V16+(V8-V16)*2/8.9	V46	V47+(V40-V47)*1.2/7.4
V15	V16+(V8-V16)*1/8.9	V47	VINN8
V16	VINN5	V48	V55+(V47-V55)*9.7/10.7
V17	V23+(V16-V23)*6.2/7.4	V49	V55+(V47-V55)*8.6/10.7
V18	V23+(V16-V23)*5/7.4	V50	V55+(V47-V55)*7.4/10.7
V19	V23+(V16-V23)*4/7.4	V51	V55+(V47-V55)*6.1/10.7
V20	V23+(V16-V23)*3/7.4	V52	V55+(V47-V55)*4.7/10.7
V21	V23+(V16-V23)*2/7.4	V53	V55+(V47-V55)*3.2/10.7
V22	V23+(V16-V23)*1/7.4	V54	V55+(V47-V55)*1.6/10.7
V23	VINN6	V55	VINN9
V24	V40+(V23-V40)*16.1/17.1	V56	V57+(V55-V57)*1/2
V25	V40+(V23-V40)*15/17.1	V57	VINN10
V26	V40+(V23-V40)*14/17.1	V58	VINN11
V27	V40+(V23-V40)*13/17.1	V59	V62+(V58-V62)*10.5/13
V28	V40+(V23-V40)*12/17.1	V60	V62+(V58-V62)*7.5/13
V29	V40+(V23-V40)*11/17.1	V61	V62+(V58-V62)*4/13
V30	V40+(V23-V40)*10/17.1	V62	VINN12
V31	V40+(V23-V40)*9/17.1	V63	VINN13

Table 5.10.4.2.3 Gamma Adjusting Voltage Formula (Negative polarity)

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINP0	V32	V40+(V23-V40)*8/17.1
V1	VINP1	V33	V40+(V23-V40)*7/17.1
V2	V5+(V1-V5)*(9/13)	V34	V40+(V23-V40)*6/17.1
V3	V5+(V1-V5)*(6/13)	V35	V40+(V23-V40)*5/17.1
V4	V5+(V1-V5)*(2.5/13))	V36	V40+(V23-V40)*4/17.1
V5	VINP2	V37	V40+(V23-V40)*3/17.1
V6	VINP3	V38	V40+(V23-V40)*217.1
V7	V8+(V6-V8)*1/2	V39	V40+(V23-V40)*1/17.1
V8	VINP4	V40	VINP7
V9	V16+(V8-V16)*7.6/8.9	V41	V47+(V40-V47)*6.4/7.4
V10	V16+(V8-V16)*6.3/8.9	V42	V47+(V40-V47)*5.4/7.4
V11	V16+(V8-V16)*5/8.9	V43	V47+(V40-V47)*4.4/7.4
V12	V16+(V8-V16)*4/8.9	V44	V47+(V40-V47)*3.4/7.4
V13	V16+(V8-V16)*3/8.9	V45	V47+(V40-V47)*2.4/7.4
V14	V16+(V8-V16)*2/8.9	V46	V47+(V40-V47)*1.2/7.4
V15	V16+(V8-V16)*1/8.9	V47	VINP8
V16	VINP5	V48	V55+(V47-V55)*9.7/10.7
V17	V23+(V16-V23)*6.2/7.4	V49	V55+(V47-V55)*8.6/10.7
V18	V23+(V16-V23)*5/7.4	V50	V55+(V47-V55)*7.4/10.7
V19	V23+(V16-V23)*4/7.4	V51	V55+(V47-V55)*6.1/10.7
V20	V23+(V16-V23)*3/7.4	V52	V55+(V47-V55)*4.7/10.7
V21	V23+(V16-V23)*2/7.4	V53	V55+(V47-V55)*3.2/10.7
V22	V23+(V16-V23)*1/7.4	V54	V55+(V47-V55)*1.6/10.7
V23	VINP6	V55	VINP9
V24	V40+(V23-V40)*16.1/17.1	V56	V57+(V55-V57)*1/2
V25	V40+(V23-V40)*15/17.1	V57	VINP10
V26	V40+(V23-V40)*14/17.1	V58	VINP11
V27	V40+(V23-V40)*13/17.1	V59	V62+(V58-V62)*10.5/13
V28	V40+(V23-V40)*12/17.1	V60	V62+(V58-V62)*7.5/13
V29	V40+(V23-V40)*11/17.1	V61	V62+(V58-V62)*4/13
V30	V40+(V23-V40)*10/17.1	V62	VINP12
V31	V40+(V23-V40)*9/17.1	V63	VINP13

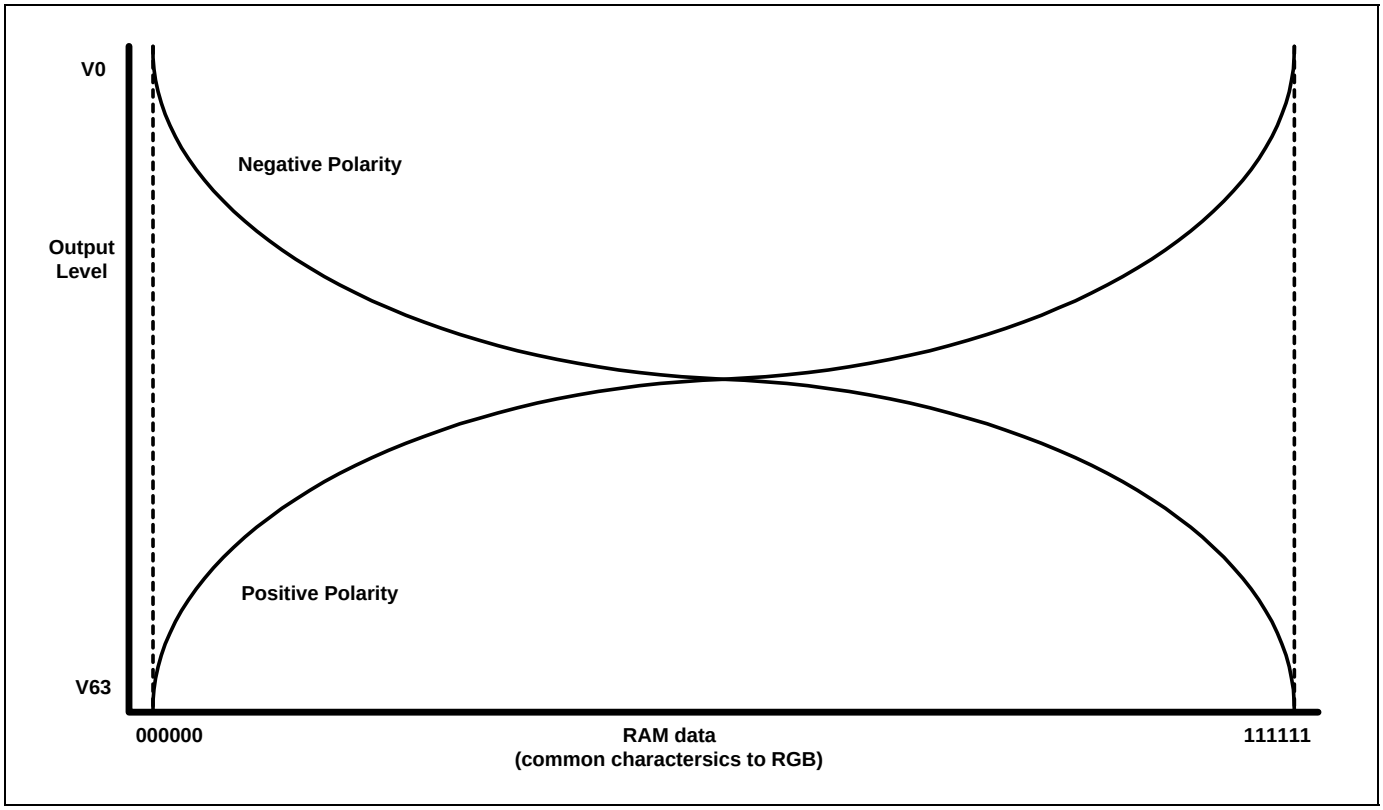


Figure 5.10.4.2.1 Relationship between RAM data and output voltage

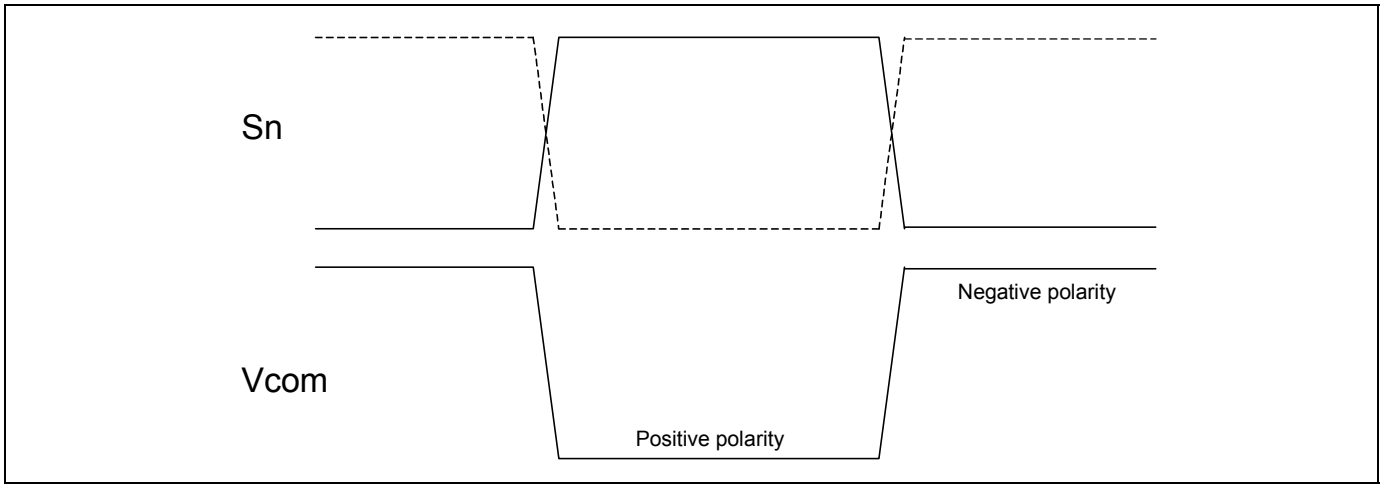


Figure 5.10.4.2.2 Relationship between source output and Vcom

6. RESET

If the /RESET input becomes low (“0”), the internal timing generator is initialized. The reset command will also initialize each register to its default value. These default values are listed in the table below (Register number is an estimate. Understand that there is a case where it changes later).

Register		Reset Command	Default Value
Driver output control(R01H)	R01	O	0027H
LCD-Driving-waveform control (R02H)	R02	O	0003H
Entry mode(R03H)	R03	O	0003H
Oscillator control (R04h)	R04	O	2801H
Display control (R07H)	R07	O	0000H
Blank period control 1 (R08H)	R08	O	0404H
Frame cycle control 1 (R0AH)	R0A	O	000BH
Frame cycle control (R0BH)	R0B	O	0003H
External interface control(R0CH)	R0C	O	0000H
Power control 1 (R10H)	R10	O	0000H
Power control 2 (R11H)	R11	O	0004H
Power control 3 (R12H)	R12	O	0033H
Power control 4 (R13H)	R13	O	0C00H
Power control 5 (R14H)	R14	O	0000H
Power control 6 (R15H)	R15	O	0000H
Power control 7 (R16H)	R16	O	0006H
RAM address set 1 (R20H)	R20	O	0000H
RAM address set 2 (R21H)	R21	O	0000H
Gamma control 1 (R30H)	R30	O	0000H
Gamma control 2 (R31H)	R31	O	0000H
Gamma control 3 (R32H)	R32	O	0000H
Gamma control 4 (R33H)	R33	O	0000H
Gamma control 5 (R34H)	R34	O	0000H
Gamma control 6 (R35H)	R35	O	0000H
Gamma control 7 (R36H)	R36	O	0000H
Gamma control 8 (R37H)	R37	O	0000H
Gamma control 9 (R38H)	R38	O	0000H
Gamma control 10 (R39H)	R39	O	0000H
Gamma control 11 (R3AH)	R3A	O	0000H
Gamma control 12 (R3BH)	R3B	O	0000H
Gamma control 13 (R3CH)	R3C	O	0000H
Gamma control 14 (R3DH)	R3D	O	0000H
Vertical scroll control (R41H)	R41	O	0000H
1st screen driving position (R42H)	R42	O	013FH
1st screen driving position (R43H)	R43	O	0000H
2nd screen driving position (R44H)	R44	O	013FH
2nd screen driving position (R45H)	R45	O	0000H
Horizontal window address (R46H)	R46	O	EF00H
Vertical window Address (R47H)	R47	O	013FH
Vertical window Address (R48H)	R48	O	0000H
MDDI wake up control (R50h)	R50	O	0000H
MDDI Link wake-up start position (R51h)	R51	O	0000H
Sub panel control 1 (R52H)	R52	O	000AH
Sub panel control 2 (R53h)	R53	O	007AH
Sub panel control 3 (R54h)	R54	O	0022H
GPIO value(R55H)	R55	O	0000H
GPIO in/output control(R56H)	R56	O	0000H
GPIO Clear(R57H)	R57	O	0000H
GPIO interrupt enable(R58H)	R58	O	0000H
GPIO polarity selection (R59H)	R59	O	03FFH

MTP INIT(R60h)	R60	O	0005H
MTP VCOMH read(R61h)	R61	O	0000H
Set MTP Test Key(R62h)	R62	O	0000H
Timing of signal from GOE (R70h)	R70	O	010BH
Gate start pulse delay timing (R71h)	R71	O	0000H
RED output start timing (R72h)	R72	O	0001H
GREEN output start timing (R73h)	R73	O	0003H
BLUE output start timing (R74h)	R74	O	0003H
RSW timing (R75h)	R75	O	0102H
GSW timing (R76h)	R76	O	0102H
BSW timing (R77h)	R77	O	0102H
Vcom Output Control (R78h)	R78	O	0000H
Panel signal control 1 (R79h)	R79	O	0000H
Panel signal control2 (R7Ah)	R7A	O	0000H
GATE1, 2 Switching control(R97h)	R97	O	0000H

NOTE: O: Default value set, X: Default value not set

7. COMMANDS

7.1 INSTRUCTION TABLE

Reg. No	R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0	Register Name / Description
IR	0	0	0	0	0	0	0	0	0	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	**Index /** Sets the index register value
SR	1	0	0	0	0	0	0	0	0	L8	L7	L6	L5	L4	L3	L2	L1	L0	**Status read /** Reads the internal status of the S6D1121
R00h	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Production code
	1	1	0	0	0	1	0	0	0	1	0	0	1	0	0	0	0	1	**Production code read /** Production code
R01h	0	1	VSPL	HSPL	DPL	EPL	0	0	0	SS	0	0	NL5	NL4	NL3	NL2	NL1	NL0	**Driver output control(R01H) /** VSPL: set polarity of VSYNC pin. HSPL: set polarity of HSYNC pin. DPL: set polarity of DOTCLK pin. EPL: set polarity of ENABLE pin SS: source driver shift direction NL5-0: number of driving lines
R02h	0	1	0	0	0	0	0	0	0	GUD	0	SINV	FLD1	FLD0	0	0	B/C	EOR	**LCD-Driving-waveform control (R02H)/** GUD: set the gate direction SINV: inverts the polarity of source output FLD1-0: number of interlaced field B/C: LCD drive AC waveform EOR: Exclusive OR-ing the AC waveform
R03h	0	1	TRI	DFM	0	BGR	0	0	0	0	0	0	0	0	AM	0	I/D1	I/D0	**Entry mode(R03H) /** TRI : 8-bit interface mode DFM: defines color depth for the IC BGR: RGB swap control AM: Set the automatic update method of the AC I/D1-0: address counter Increment / Decrement control
R04h	0	1	0	0	RADJ 5	RADJ 4	RADJ 3	RADJ 2	RADJ 1	RADJ 0	0	0	0	0	0	0	0	OSC_O N	**Oscillator control (R04h)/** RADJ5-0 : Osc freq select OSC_ON : start oscillation
R07h	0	1	PT1	PT0	VLE2	VLE1	0	0	0	SPT	0	GON	CL	REV	0	0	D1	D0	**Display control (R07H) /** PT1-0: Non-display area source output control VLE2-1: 1st /2nd partial vertical scroll SPT: 1st /2nd partial display enable GON: gate on/off control CL: 8-color display mode enable REV: display area inversion drive D1-0: source output control
R08h	0	1	FMP1	FMP0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0	**Blank period control 1 (R08H)/** FMP1-0: set the output timing of frame cycle signal FP3-0: Front porch setting BP3-0: Back porch setting
R0Ah	0	1	0	0	0	0	ECS3	ECS2	ECS1	ECS0	0	0	0	RTN4	RTN3	RTN2	RTN1	RTN0	**Frame cycle control 1 (R0AH)/** ECS3-0: VCI recycling period setting. RTN5-0: set the 1-H period
R0Bh	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	DCR2	DCR1	DCR0	**Frame cycle control (R0BH)/** DCR2-0:Set clock cycle for step-up circuit.
R0Ch	0	1	0	0	0	0	0	0	0	0	0	RM	DM1	DM0	0	0	RIM1	RIM0	**External interface control(R0CH) /** RM: specify the interface for RAM access DM1-0: specify display operation mode RIM1-0: specify RGB-I/F mode
R10h	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SLP	STB	**Power control 1 (R10H) /** SLP: sleep mode control STB: standby mode control
R11h	0	1	0	0	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0	0	VCI1_ OFF	0	0	0	0	VC1	VC0	**Power control 2 (R11H)/** VRH5-0:set GVDD voltage VCI1_OFF:control VCI1 voltage generation VC1-0:set VCI1 voltage
R12h	0	1	0	0	0	0	0	0	0	0	0	SAP2	SAP1	SAP0	0	DC2	DC1	DC0	**Power control 3 (R12H) /** SAP2-0:Adjust fixed current DC2-0:Adjust the frequency
R13h	0	1	VR2C 3	VR2C 2	VR2C 1	VR2C 0	VR1C 3	VR1C 2	VR1C 1	VR1C 0	VGLRC 4	VGLR C3	VGLR C2	VGLR C1	VGLR C0	PON	PON1	AON	**Power control 4 (R13H)/** VR2C4~0: set the VR2 voltage VR1C4~0: set the VR1 voltage VGLRC4~0:set the VGLR voltage PON: booster circuit control PON1: booster circuit control AON: operation start bit for the amplifier.
R14h	0	1	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	0	0	VML5	VML4	VML3	VML2	VML1	VML0	**Power control 5 (R14H)/** VCM5-0:set the VCOMH voltage VML4-0:set the amplitude of VCOM voltage
R15h	0	1	VCM R	0	VMA5	VMA4	VMA3	VMA2	VMA1	VMA0	0	0	VMH5	VMH4	VMH3	VMH2	VMH1	VMH0	**Power control 6 (R15H)/** VCMR: VCOMH control by VCOMR pin VMA5-0:set the VCOMH voltage (coupling) VMH5-0:set the VCOMH voltage (direct)
R16h	0	1	0	0	0	0	0	0	0	0	VCOM_ OFF	0	0	0	0	PREC	COMS	COMA	**Power control 7 (R17H)/** VCOM_OFF: control on/off the VCOM, VCOMPREC and VCOMDC. PREC: control the pre-charge for coupling VCOM driving method COMS: selection the VCOM driving method COMA: setup VcomL voltage
R20h	0	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	**Write data to GRAM (R20H)/(R21H)** AD16-0:Input data for GRAM
R21h	0	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	

R22h	0	1	WD17-0 : Pin assignment varies according to the interface method															**Write data to GRAM (R22H)/** WD17-0:Input data for GRAM
	1	1	RD17-0 : Pin assignment varies according to the interface method															**Read data from GRAM (R22H)/** RD17-0:Read data from GRAM
R30h	0	1	0	0	PKP1[5:0]						0	0	PKP0[5:0]					**Gamma control 1 (R30H)/** Adjust Gamma voltage
R31h	0	1	0	0	PKP3[5:0]						0	0	PKP2[5:0]					**Gamma control 2 (R31H)/** Adjust Gamma voltage
R32h	0	1	0	0	PKP5[5:0]						0	0	PKP4[5:0]					**Gamma control 3 (R32H)/** Adjust Gamma voltage
R33h	0	1	0	0	PKP7[5:0]						0	0	PKP6[5:0]					**Gamma control 4 (R33H)/** Adjust Gamma voltage
R34h	0	1	0	0	PKP9[5:0]						0	0	PKP8[5:0]					**Gamma control 5 (R34H)/** Adjust Gamma voltage
R35h	0	1	0	0	PKP11[5:0]						0	0	PKP10[5:0]					**Gamma control 6 (R35H)/** Adjust Gamma voltage
R36h	0	1	0	0	PKN1[5:0]						0	0	PKN0[5:0]					**Gamma control 7 (R36H)/** Adjust Gamma voltage
R37h	0	1	0	0	PKN3[5:0]						0-	0	PKN2[5:0]					**Gamma control 8 (R37H)/** Adjust Gamma voltage
R38h	0	1	0	0	PRN5[5:0]						0	0	PRN4[5:0]					**Gamma control 9 (R38H)/** Adjust Gamma voltage
R39h	0	1	0	0	PKN7[5:0]						0-	0	PKN6[5:0]					**Gamma control 10 (R39H)/** Adjust Gamma voltage
R3Ah	0	1	0	0	PRN9[5:0]						0	0	PRN8[5:0]					**Gamma control 11 (R3AH)/** Adjust Gamma voltage
R3Bh	0	1	0	0	PRN11[5:0]						0	0	PRN10[5:0]					**Gamma control 12 (R3BH)/** Adjust Gamma voltage
R3Ch	0	1	0	0	0	VRP1[4:0]					0	0	0	VRP0[4:0]				**Gamma control 13 (R3CH)/** Adjust Amplitude voltage
R3Dh	0	1	0	0	0	VRN1[4:0]					0	0	0	VRN0[4:0]				**Gamma control 14 (R3DH)/** Adjust Amplitude voltage
R41h	0	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	**Vertical scroll control (R41H)/** VL8-0:
R42h	0	1	0	0	0	0	0	0	0	SE18	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	**1st screen driving position (R42H, R43H)** SE18-10: 1st screen end position SS18-10: 1st screen start position
R43h	0	1	0	0	0	0	0	0	0	SS18	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10	
R44h	0	1	0	0	0	0	0	0	0	SE28	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	**2nd screen driving position (R44H, R45H)** SE28-20: 2nd screen end position SS28-20: 2nd screen start position
R45h	0	1	0	0	0	0	0	0	0	SS28	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20	
R46h	0	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0	**Horizontal window address (R46H)** HSA7-0: Horizontal window address start position HEA7-0: Horizontal window address end position
R47h	0	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	**Vertical window Address (R47H, R48H)** VEA8-0: Vertical window address end position VSA8-0: Vertical window address start position
R48h	0	1	0	0	0	0	0	0		VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	
R50h	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	WAKE_EN	MDDI wake up control (R50h)/ When VWAKE_EN = 1, client initiated wakeup is enabled.
R51h	0	1	WKL7	WKL6	WKL5	WKL4	WKL3	WKL2	WKL1	WKL0	0	0	0	0	WKF3	WKF2	WKF1	WKF0	**MDDI Link wake-up start position (R51h)/** WKF : The frame that data is written WKL : The line that data is written
R52h	0	1	0	0	0	0	0	0	0	0	0	0	0	0	MODE_SEL[1:0]		SUB_IM[1:0]		**Sub panel control 1 (R52H)/** SUB_IM[1-0] : bus width MODE_SEL [1:0]: STN, MPU interface
R53h	0	1	0	0	0	0	0	0	0	0	SUB_SEL								**Sub panel control 2 (R53h)/ Sub panel selection index** SUB_SEL: select main/sub panel
R54h	0	1	0	0	0	0	0	0	0	0	SUB_WR								**Sub panel control 3 (R54h)/** SUB_WR: GRAM write data sub frame
R55h			0	0	0	0	0	0	GPIO_DATA[9:0]										**GPIO value(R55H)** GPIO_DATA 9-0
R56h			0	0	0	0	0	0	GPIO_CON[9:0]										**GPIO in/output control(R56H)** GPIO_CON 9-0
R57h			0	0	0	0	0	0	GPIO_CLR[9:0]										**GPIO Clear(R57H)** GPIO_CLR 9-0
R58h			0	0	0	0	0	0	GPIO_EN[9:0]										**GPIO interrupt enable(R58H)** GPIO_EN 9-0
R59h			0	0	0	0	0	0	GPIO_POL[9:0]										**GPIO polarity selection (R59H)** GPIO_POL 9-0
R60h	0	1	0	0	0	0	0	0	0	0	0	0	0	0	MTP_LOAD	MTP_WRB	MTP_SEL	MTP_ERB	**MTP INIT(R60h)** MTP_LOAD: MTP data load. MTP_WRB: MTP program enable signal MTP_SEL : VCOMH selection MTP_ERB: MTP initial mode control
R61h	0	1	0	0	0	0	0	0	0	0	0	MTP_D[6:0]							**MTP VCOMH read(R61h)** Dummy:
R62h	0	1	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	**Set MTP Test Key(R62h)** 8Ch
R70h	0	1	0	0	0	0	0	0	GOST[1:0]		0	0	0	GOED[4:0]					**Timing of signal from GOE (R70h)/** GOST[1:0] : start timing GOED[4:0] : end timing

R71h	0	1	0	0	0	0	0	0	0	0	0	0	0	0	GSP_DLY[3:0]				**Gate start pulse delay timing (R71h)/** GSP_DLY3-0 : gate start pulse delay
R72h	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	R_STP[2:0]			**RED output start timing (R72h)/** R_STP[2:0] : RED output start timing
R73h	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	G_STP[2:0]			**GREEN output start timing (R73h)/** G_STP[2:0] : GREEN output start timing
R74h	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	B_STP[2:0]			**BLUE output start timing (R74h)/** B_STP[2:0] : BLUE output start timing
R75h	0	1	0	0	0	0	0	0	M_RSTP[1:0]		0	0	0	0	0	M_RPW[2:0]			**RSW timing (R75h)/** M_RSTP1-0 : start timing of RSW M_RPW2-0 : pulse width timing of RSW
R76h	0	1	0	0	0	0	0	0	M_GSTP[1:0]		0	0	0	0	0	M_GPW[2:0]			**GSW timing (R76h)/** M_GSTP1-0 : start timing of GSW M_GPW2-0 : pulse width timing of GSW
R77h	0	1	0	0	0	0	0	0	M_BSTP[1:0]		0	0	0	0	0	M_BPW[2:0]			**BSW timing (R77h)/** M_BSTP-0 : start timing of BSW M_BPW2-0 : pulse width timing of BSW
R78h	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VMCHG[1:0]		**Vcom Output Control (R78h)** VMCHG1-0 : starting time of Vcom output
R79h	0	1	0	0	LGSP_OFF	LGCLK4_OFF	LGCLK3_OFF	LGCLK2_OFF	LGCLK1_OFF	0	RGSP_OFF	RGCLK4_OFF	RGCLK3_OFF	RGCLK2_OFF	RGCLK1_OFF	R_OFF	G_OFF	B_OFF	**Panel signal control 1 (R79h)/** LGSP_OFF : GSP output control LGCLK4_OFF : GCLK4 output control LGCLK3_OFF : GCLK3 output control LGCLK2_OFF : GCLK2 output control LGCLK1_OFF : GCLK1 output control RGSP_OFF : GSP output control RGCLK4_OFF : GCLK4 output control RGCLK3_OFF : GCLK3 output control RGCLK2_OFF : GCLK2 output control RGCLK1_OFF : GCLK1 output control R_OFF : RSW output control G_OFF : GSW output control B_OFF : BSW output control
R7Ah	0	1	0	0	LGSP_POL	LGCLK4_POL	LGCLK3_POL	LGCLK2_POL	LGCLK1_POL	0	RGSP_POL	RGCLK4_POL	RGCLK3_POL	RGCLK2_POL	RGCLK1_POL	R_POL	G_POL	B_POL	**Panel signal control2 (R7Ah)/** LGSP_POL : GSP polarity control LGCLK4_POL : GCLK4 polarity control LGCLK3_POL : GCLK3 polarity control LGCLK2_POL : GCLK2 polarity control LGCLK1_POL : GCLK1 polarity control RGSP_POL : GSP polarity control RGCLK4_POL : GCLK4 polarity control RGCLK3_POL : GCLK3 polarity control RGCLK2_POL : GCLK2 polarity control RGCLK1_POL : GCLK1 polarity control R_POL : RSW polarity control G_POL : GSW polarity control B_POL : BSW polarity control
R90h	0	1	Test command1																**Don't use this command**
R91h ~ R96h	0	1	Test command2																**Don't use this command**
R97h	0	1	0	0	0	0	0	0	0	0	CHNG	0	0	0	0	0	0	0	**CHNG : Swap GCLK1 and GCLK2**

7.2 INSTRUCTION DESCRIPTION

Production Code (R00H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R	1	0	0	0	1	0	0	0	1	0	0	1	0	0	0	0	1
default	0	0	0	0	1	0	0	0	1	0	0	1	0	0	0	0	1

If this register is read forcibly, *1121h is read.

Driver Output Control (R01H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	VSPL	HSPL	DPL	EPL	0	0	0	SS	0	0	NL5	NL4	NL3	NL2	NL1	NL0
default	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1

VSPL: reverses the polarity of the VSYNC signal.

VSPL= “0”: VSYNC is low active.

VSPL= “1”: VSYNC is high active.

HSPL: reverses the polarity of the HSYNC signal.

HSPL= “0”: HSYNC is low active.

HSPL= “1”: HSYNC is high active.

DPL: reverses the polarity of the DOTCLK signal.

DPL= “0”: Display data is fetched on the rising edge of DOTCLK.

DPL= “1”: Display data is fetched on the falling edge of DOTCLK.

EPL: Set the polarity of ENABLE pin while using RGB interface.

EPL = “0”: ENABLE = ”Low” / write data of PD17-0

ENABLE = ”High” / don’t write data of PD17-0

EPL = “1”: ENABLE = ”High” / write data of PD17-0

ENABLE = ”Low” / don’t write data of PD17-0

SS: Selects the output shift direction of the source driver. When SS = 0, S1 shifts to S240. When SS = 1, S240 shifts to S1. In addition, SS and BGR bits should be specified in case of any change in the RGB order.

NL5–0: Specify the number of raster-rows to be driven. The number of raster-row can be adjusted in units of eight. The address mapping of GRAM is independent of this setting. The set value should be higher than the panel size.

Table 7.2.1 NL bit and Driver Duty

NL5	NL4	NL3	NL2	NL1	NL0	Display Size	LCD Raster Rows	Gate- Lines Used
0	0	0	0	0	0	Setting disabled	Setting disabled	Setting disabled
0	0	0	0	0	1	240RGB X 16	16	G1 to G16
0	0	0	0	1	0	240RGB X 24	24	G1 to G24
0	0	0	0	1	1	240RGB X 32	32	G1 to G32
0	0	0	1	0	0	240RGB X 40	40	G1 to G40
0	0	0	1	0	1	240RGB X 48	48	G1 to G48
0	0	0	1	1	0	240RGB X 56	56	G1 to G56
0	0	0	1	1	1	240RGB X 64	64	G1 to G64
0	0	1	0	0	0	240RGB X 72	72	G1 to G72
0	0	1	0	0	1	240RGB X 80	80	G1 to G80
0	0	1	0	1	0	240RGB X 88	88	G1 to G88
0	0	1	0	1	1	240RGB X 96	96	G1 to G96
0	0	1	1	0	0	240RGB X 104	104	G1 to G104
0	0	1	1	0	1	240RGB X 112	112	G1 to G112
0	0	1	1	1	0	240RGB X 120	120	G1 to G120
0	0	1	1	1	1	240RGB X 128	128	G1 to G128
0	1	0	0	0	0	240RGB X 136	136	G1 to G136
0	1	0	0	0	1	240RGB X 144	144	G1 to G144
0	1	0	0	1	0	240RGB X 152	152	G1 to G152
0	1	0	0	1	1	240RGB X 160	160	G1 to G160
0	1	0	1	0	0	240RGB X 168	168	G1 to G168
0	1	0	1	0	1	240RGB X 176	176	G1 to G176
0	1	0	1	1	0	240RGB X 184	184	G1 to G184
0	1	0	1	1	1	240RGB X 192	192	G1 to G192
0	1	1	0	0	0	240RGB X 200	200	G1 to G200
0	1	1	0	0	1	240RGB X 208	208	G1 to G208
0	1	1	0	1	0	240RGB X 216	216	G1 to G216
0	1	1	0	1	1	240RGB X 224	224	G1 to G224
0	1	1	1	0	0	240RGB X 232	232	G1 to G232
0	1	1	1	0	1	240RGB X 240	240	G1 to G240
0	1	1	1	1	0	240RGB X 248	248	G1 to G248
0	1	1	1	1	1	240RGB X 256	256	G1 to G256
1	0	0	0	0	0	240RGB X 264	264	G1 to G264
1	0	0	0	0	1	240RGB X 272	272	G1 to G272
1	0	0	0	1	0	240RGB X 280	280	G1 to G280
1	0	0	0	1	1	240RGB X 288	288	G1 to G288
1	0	0	1	0	0	240RGB X 296	296	G1 to G296
1	0	0	1	0	1	240RGB X 304	304	G1 to G304
1	0	0	1	1	0	240RGB X 312	312	G1 to G312
1	0	0	1	1	1	240RGB X 320	320	G1 to G320

NOTE: A FP (front porch) and BP (back porch) period will be inserted as blanking period (All gates output VGL level) before / after the driver scan through all of the scans

LCD Driving Waveform Control (R02H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	0	0	0	0	0	0	0	GUD	0	SINV	FLD 1	FLD 0	0	0	B/C	EOR
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

NOTES:

1. FLD function is not available when the external display interface (i.e. RGB) is in use.
2. The 2-line interlaced display is functioned by FLD=11.
3. On the 2 phase gate clock method, the GCLK3B and GCLK4B are used for the generation of VCOM signal in the LTPS panel.

GUD: This bit is for the gate scan direction. See the following table for the set up value.

Table 7.2.2 Association and function chart for scanning FLD, GUD

FLD[1:0]	GUD	Scanning method and Gate clock direction
00	0	Forward scan direction: G1 → G2 → G3 →……. → G320 → G1 → G2 → … Forward gate clock direction: GSPB/GCLK2B → GCLK1B → GCLK2B → GCLK1 …… (1st Frame), Frame end (dummy 3 line over),. GSPB/GCLK2B → GCLK1B → GCLK2B → ……. … (2nd Frame) Forward Vcom clock direction: GCLK4B → GCLK3B → GCLK4B → GCLK3B ….. (1st Frame), Frame end (dummy 3 line over),. GSPB/GCLK3B → GCLK4B → GCLK3B → ……..… (2nd Frame)
	1	Backward scan direction: G320 → G319 → G318 → ……. → G1 → G320 → G319 → … Backward gate clock direction: GSPB/ GCLK1B → GCLK2B → GCLK1B → ……..... (1st Frame), Frame end (dummy 3 line over),. GSPB/GCLK1B → GCLK2B → GCLK1B→ …… (2nd Frame) Backward Vcom clock direction: GSPB/ GCLK3B → GCLK4B → GCLK3B → …….. (1st Frame), Frame end (dummy 3 line over),. GSPB/GCLK4B → GCLK3B → GCLK4B → ….... (2nd Frame)
01	0	Forward scan direction : G1 → G2 → G3 → ……. → G320 → G1 → G2 → … Forward gate clock direction : GCLK1B → GCLK2B → GCLK3B → GCLK4B → GCLK1B → …
	1	Backward scan direction : G320 → G319 → G318 → ……. → G1 → G320 → G319 → … Backward gate clock direction : GCLK4B → GCLK3B → GCLK2B → GCLK1B → GCLK4B → …
10	0	Forward scan direction: G1 → G2 → G3 →……. → G320 → G1 → G2 → G3 →…… Forward gate clock direction: LGSPB/LGCLK4B → RGSPB/RGCLK4B → LGCLK1B → RGCLK1B → LGCLK2B → RGCLK2B → ……. Frame end (dummy 6 line over), LGSPB/LGCLK4B → RGSPB/RGCLK4B → LGCLK1B → …
	1	Backward scan direction: G320 → G319 → G318 →……. → G1 → G320 → G319 →…… Backward gate clock direction: RGSPB/RGCLK1B → LGSPB/LGCLK1B → RGCLK4B → LGCLK4B → RGCLK3B → LGCLK3B → ……. Frame end (dummy 6 line over), RGSPB/RGCLK1B → LGSPB/LGCLK1B → RGCLK4B → ……
11	0	Forward scan direction: G1 → G3 → G5 →……. → G319 → G2 → G4 → G6 → … G320 → … Forward gate clock direction: LGSPB/LGCLK4B → LGCLK1B/RGCLK1B → LGCLK2B/GCLK2B → LGCLK3B/RGCLK3B → LGCLK4B/RGCLK4B → …. Frame end (dummy 3 line over), RGSPB/RGCLK4B → RGCLK1B/LGCLK1B → RGCLK2B/LGCLK2B →…
	1	Backward scan direction: G320 → G318 → G316 → …. → G2 → G319 → G317 → … G1 → … Backward gate clock direction: RGSPB/RGCLK1B → RGCLK4B/LGCLK4B →RGCLK3B/ LGCLKB→ RGCLK2B/LGCLK2B → RGCLK1B/LGCLK1B → …. Frame end (dummy 3 line over), LGSPB/LGCLK1B → LGCLK4B/RGCLK4B → LGCLK3B/RGCLK3B →…

SINV: Inverts the polarity of source output value when FLD = 00 (2 phase gate drive method).

Table 7.2.3 SINV Function Description

SINV	Function
0	Source output data follows the polarity of GCLK3B
1	Source output data follows the polarity of GCLK4B

FLD[1:0]: These bits are for the set up of the interlaced driver's n raster-row. See the following table and figure for the set up value, field raster-row and scanning method.

Table 7.2.4 Association chart for scanning FLD and n raster-row

FLD [1:0]	Scanning method
00	1 field, 2 phase gate driving mode
01	1 field, 4 phase gate driving mode
10	2 field (normal mode), 4 phase gate driving mode
11	2 field (interlaced mode), 4 phase gate driving mode

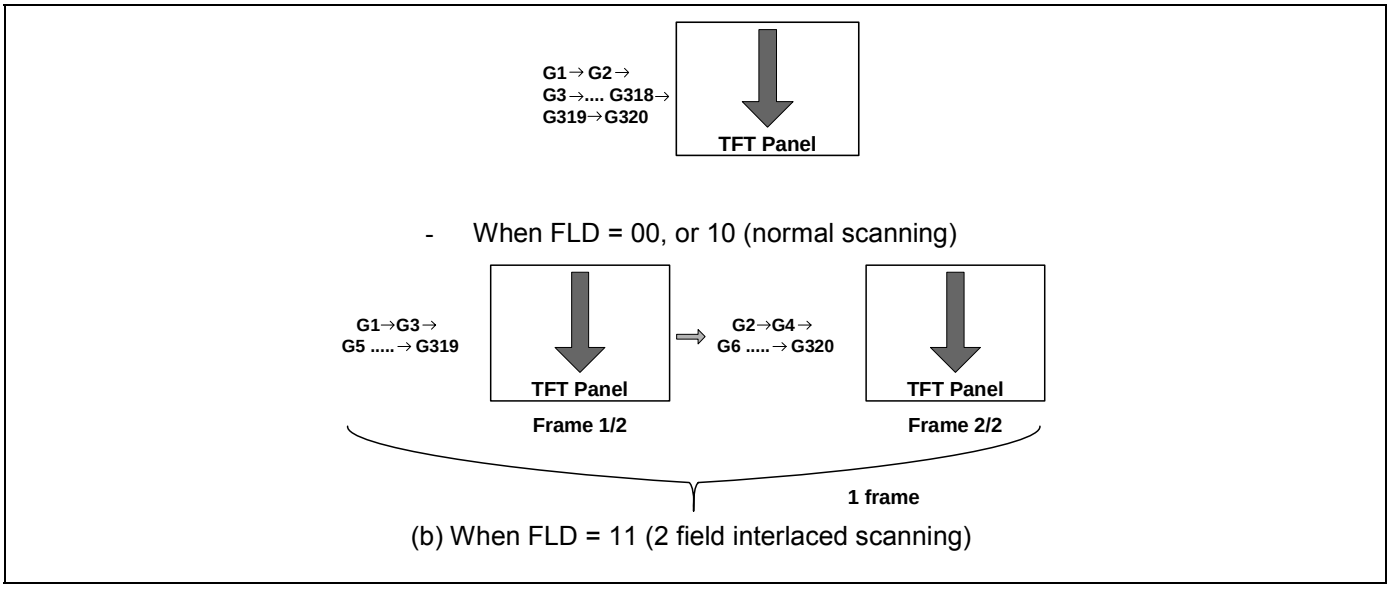


Figure 7.2.1 Interlaced Scanning Method

B/C: When B/C = 0, a frame inversion waveform is generated and it alternates at every frame. When B/C = 1, n raster-row AC waveform is generated and alternates in each raster-row specified by bits EOR in the LCD-driving-waveform control register (R02h).

EOR: When the line inversion waveform is set (B/C = 1) and EOR = 1, the odd/even frame-select signals is selected, and the n-raster-row reversed signals are being Exclusive-OR'ed (EOR) for alternating drive. When the EOR is used, the number of the LCD drive raster-row and the n raster-row alternates the LCD.

B/C, EOR	Inversion
0 0	Frame Inversion
0 1	Setting Prohibit
1 0	1-line inversion only
1 1	1-line inversion with frame inversion

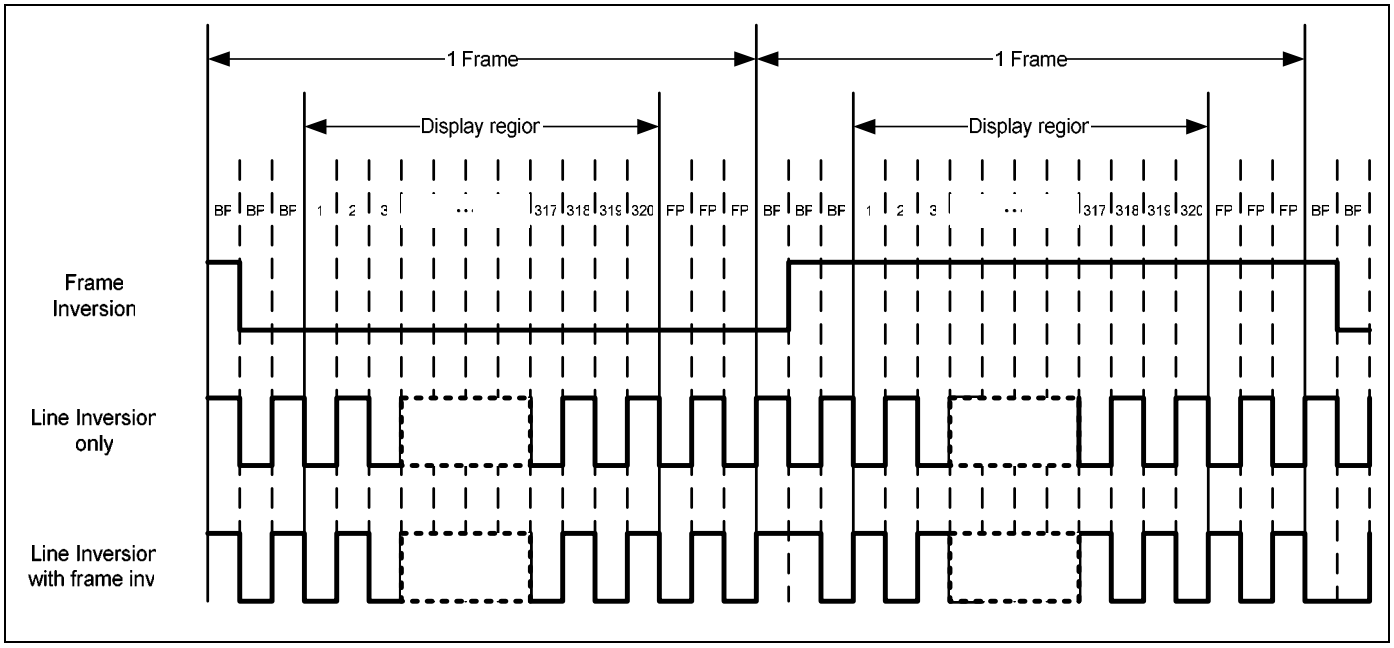


Figure 7.2.2 Frame / Line Inversion Timing

Entry Mode (R03H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	TRI	DFM	0	BGR	0	0	0	0	0	0	0	0	AM	0	I/D1	I/D0
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

TRI: This bit is active on the 80-system of 8-bit bus interface and the data for 1-pixel is transported to the memory for 3 write cycles. This bit is on the 80-system of 16-bit interface and the data for 1-pixel is transported to the memory for 2 write cycles. When the 80-system interface mode is not set in the 8-bit or16-bit mode, set TRI bit to be “0”.

DFM: When 8-bit or 16-bit 80 interface mode and TRI bit =1, DFM defines color depth for the IC.
16-bit (80-system), DFM = 0: 262k-color mode (16-bit, 2-bit data transfer to GRAM)
16-bit (80-system), DFM = 1: 262k-color mode (2-bit, 16-bit data transfer to GRAM)

8-bit (80-system), DFM = 0: 262k-color mode (3 times of 6-bit data transfer to GRAM)
8-bit (80-system), DFM = 1: 65k-color mode (5-bit, 6-bit, 5-bit data transfer to GRAM)

BGR: After writing 18-bit data to GRAM, it is changed from <R><G><B> into <B><G><R>.

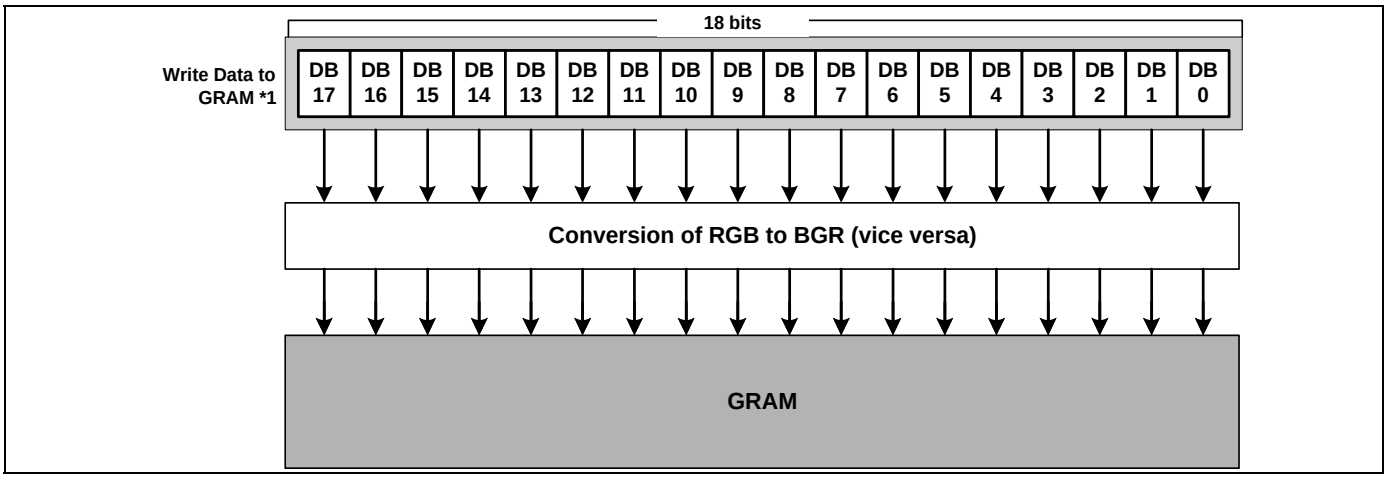


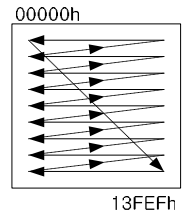
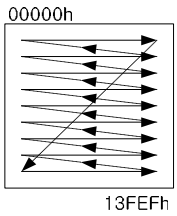
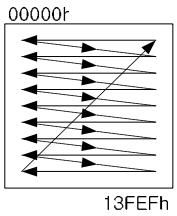
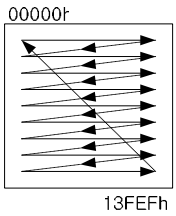
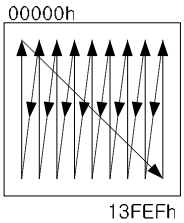
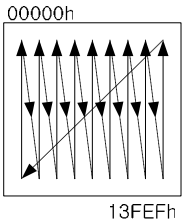
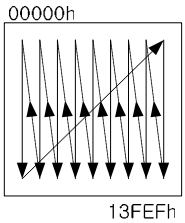
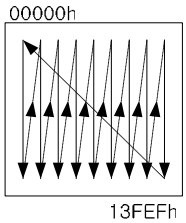
Figure 7.2.3 Write data to GRAM via RGB swapping block

This bit functions on the RGB swapping in the front of GRAM. It supports on the BGR format from CPU I/F and the BGR sub pixels of wrong manufacturing in making LTPS panel.

BGR Bit	CPU I/F Data Format	Panel Sub Pixel Structure
0	BGR	BGR
1	RGB	BGR
1	BGR	RGB
0	RGB	RGB

AM: Set the automatic update method of the AC after the data is written to GRAM. When AM = “0”, the data is continuously written in horizontally. When AM = “1”, the data is continuously written vertically. When window addresses are specified, the GRAM in the window range can be written to according to the ID[1:0] and AM.

I/D [1:0]: When ID[1], ID[0] = 1, the address counter (AC) is automatically increased by 1 after the data is written to the GRAM. When ID[1], ID[0] = 0, the AC is automatically decreased by 1 after the data is written to the GRAM. The increment/decrement setting of the address counter using ID[1:0] is done independently for the horizontal address and vertical address.

	ID[1:0] = “00” **H: decrement** **V: decrement**	**ID[1:0] = “01”** **H: increment** **V: decrement**	**ID[1:0] = “10”** **H: decrement** **V: increment**	**ID[1:0] = “11”** **H: increment** **V: increment**
AM=”0” **Horizontal Update**				
AM=”1” **Vertical Update**				

NOTE: When window addresses have been set, the GRAM can only be written within the window. When AM or ID is set, the start address should be written accordingly prior to memory write.

Oscillator Control (R04H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	0	0	RADJ5	RADJ4	RADJ3	RADJ2	RADJ1	RADJ0	0	0	0	0	0	0	0	OSC_ON
default	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1

RADJ [5:0]:

Select the oscillation frequency of internal oscillator.

RADJ[5:0]	Oscillation Speed	RADJ[5:0]	Oscillation Speed
00_0000	Setting disabled	10_0000	x0.873
00_0001	Setting disabled	10_0001	x0.888
00_0010	Setting disabled	10_0010	x0.901
00_0011	Setting disabled	10_0011	x0.915
00_0100	Setting disabled	10_0100	x0.934
00_0101	Setting disabled	10_0101	x0.945
00_0110	Setting disabled	10_0110	x0.962
00_0111	Setting disabled	10_0111	x0.977
00_1000	Setting disabled	10_1000	x1.0 Default
00_1001	x0.64	10_1001	x1.02
00_1010	x0.646	10_1010	x1.04
00_1011	x0.654	10_1011	x1.06
00_1100	x0.663	10_1100	x1.08
00_1101	x0.670	10_1101	x1.10
00_1110	x0.678	10_1110	x1.12
00_1111	x0.685	10_1111	x1.14
01_0000	x0.699	11_0000	x1.18
01_0001	x0.705	11_0001	x1.2
01_0010	x0.714	11_0010	x1.23
01_0011	x0.722	11_0011	x1.25
01_0100	x0.734	11_0100	x1.29
01_0101	x0.743	11_0101	x1.32
01_0110	x0.753	11_0110	x1.35
01_0111	x0.761	11_0111	x1.38
01_1000	x0.776	11_1000	x1.43
01_1001	x0.784	11_1001	x1.46
01_1010	x0.797	11_1010	x1.50
01_1011	x0.807	11_1011	x1.54
01_1100	x0.822	11_1100	x1.59
01_1101	x0.832	11_1101	x1.63
01_1110	x0.844	11_1110	x1.68
01_1111	x0.855	11_1111	x1.73

NOTE: Setting example: If the default oscillation frequency is 1MHz and the register setting of RADJ [5:0] is 001100, internal oscillator oscillation frequency is 1MHz x 0.663 = 663kHz.

OSC_ON: The start oscillation instruction restarts the oscillator from the Halt State in the stand-by mode. After this instruction, wait for at least 10 ms for the oscillation to stabilize before giving the next instruction. (See the Stand-by Mode section.)

Display Control 1 (R07H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	PT1	PT0	VLE 2	VLE 1	0	0	0	SPT	0	GON	CL	REV	0	0	D1	D0
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PT1-0: Normalize the source outputs when non-displayed area of the partial display is driven.

CL	PT1 *	PT0	Source Output on Non-display Area		VCOM Output on Non-display Area		Gate Clock Output for Non-display Area
			Positive	Negative	Positive	Negative	
0	0	0	VGS	VGS	VCOML	VCOML	operating
0	0	1	VGS	GVDD	VCOML	VCOMH	
0	1	0	GVDD	VGS	VCOML	VCOMH	
0	1	1	Setting prohibit				
1	0	0	AVSS	AVSS	VCOML	VCOML	operating
1	0	1	AVSS	GVDD	VCOML	VCOMH	
1	1	0	GVDD	AVSS	VCOML	VCOMH	
1	1	1	Setting prohibit				

NOTES: When FLD = '00', PT = '00' is not available. And VCOM output on the blanking area is always toggled.

VLE2–1: When VLE1 = 1, a vertical scroll is performed in the 1st screen. When VLE2 = 1, a vertical scroll is performed in the 2nd screen. Vertical scrolling on the two screens cannot be controlled at the same time.

VLE2	VLE1	2nd Screen	1st Screen
0	0	Fixed display	Fixed display
0	1	Fixed display	Scroll
1	0	Scroll	Fixed display
1	1	Setting disabled	Setting disabled

SPT: When SPT = 1, the 2-division LCD drive is performed. For details, see the SCREEN-DIVISION DRIVING FUNCTION section.

NOTES: This function is not available when the external display interface (i.e. RGB interface or VSYNC interface) is in use.

GON: Gate on/off control signal. All gate outputs are set to be gate off level when GON = 0. When GON = 1, gate driver is working: G1 to G320 output is either VGH or VGLROUT level. See the Instruction set up flow for further description on the display on/off flow.

GON	Gate Output
0	All gates off (All gates outputs are set to VGH)
1	Gate on(VGH / VGLROUT)

CL: CL = 1 selects 8-color display mode. For details, see the section on 8-COLOR DISPLAY MODE.

CL	Number of display colors
0	262,144 colors
1	8 colors

REV: When the REV = 1, all character and graphics display sections display with reversal. Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels.

REV	GRAM Data	Display Area	
		Positive	Negative
0	6'b000000	V63	V0
	:	:	:
	6'b111111	V0	V63
1	6'b000000	V0	V63
	:	:	:
	6'b111111	V63	V0

D1–0: When D1 is 1, display is on. And, when D1 is 0, display is off. When display is off, the display data remains in the GRAM, and can be re-displayed instantly by setting "D1 = 1". When D1 is 0, the display is off with the entire source outputs set to the VSS level. Because of this, the S6D1121 can control the charging current for the LCD with AC driving. Control the display on/off while control GON. For details, see the Instruction set up flow.

When D1–0 = 01, the internal display of the S6D1121 is performed although the display is off. When D1-0 = 00, the internal display operation halts and the display is off.

D1	D0	GON	Source output	Gate Output	VCOM Output	Internal display operation
0	0	0	AVSS	VGH	AVSS	Halt
0	1	1	AVSS	Operate	AVSS	Operate
1	0	1	Blank Display	Operate	Operate	Operate
1	1	1	Normal Display	Operate	Operate	Operate

NOTES:

1. Writing from MCU to GRAM is independent of D1–0.
2. In sleep and stand-by mode, D1–0 = 00. However, the register contents of D1–0 are not modified.
3. When source output is in the same phase with VCOM, white screen is displayed at normally white LCD panel

Display Control 2 (R08H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	FMP 1	FMP 0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
default	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0

The blanking period in the start and end of the display area can be defined using this register. When N-raster-row is driving, a blank period is inserted after all screens are drawn. Front and Back porch can be adjusted using FP3-0 and BP3-0 bits (R08h).

FMP1-0: Set the output timing of frame cycle signal (frame maker). When FMP [1:0] = 2'b00, a high active pulse FLM is output at the start of front porch period 1H period. Make sure of 2'b00 ≤ FMP ≤ FP + BP.

Table 7.2.5 Examples of Using FMP Function with FP and BP Bits

FMP1	FMP0	FP=1, BP=3	FP=2, BP=2	FP=3, BP=3	FP=1, BP=5
0	0	FP1	FP1	FP1	FP1
0	1	BP1	FP2	FP2	BP1
1	0	BP2	BP1	FP3	BP2
1	1	BP3	BP2	BP1	BP3

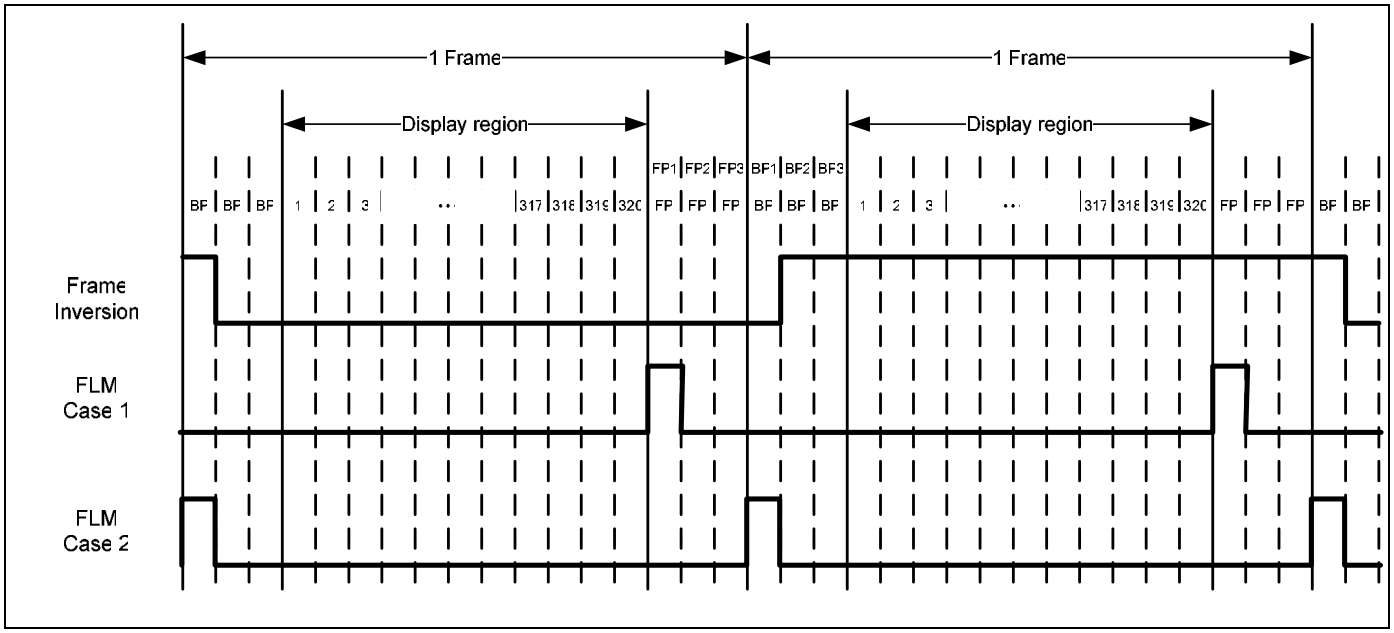


Figure 7.2.4 FLM Signal Generation Timing

NOTES:

1. In the case of starting point of first frame, the starting point of the fastest FLM signal is BP1. The other frame is normal operation.
2. From figure 7.2.4, the case1 is FMP=2'b00, and the case2 is FMP=2'b11.
3. The first waveform of FLM is always fixed on the BP1 period, and the other FLM signal is followed the setting of FMP register value.

FP3-0/BP3-0: Set the periods of blanking (the front and back porch), which are placed at the beginning and end of the display. FP3-0 is for a front porch and BP3-0 is for a back porch. When front and back porches are set, the settings should meet the following conditions.

$4 \leq BP + FP \leq 16$ raster-rows

2 Phase Gate Clock Type: $FP \geq 1$ raster-rows, $BP \geq 3$ raster-rows

4 Phase Gate Clock Type: $FP \geq 2$ raster-rows, $BP \geq 2$ raster-rows

When the external display interface is in use, the back porch (BP) will start on the falling edge of the VSYNC signal and the display operation will commence at the end of the back-porch period. The front porch (FP) will start when data for the number of raster-rows specified by the NL bits has been displayed. During the period between the completion of the front-porch period and the next VSYNC signal, the display will remain blank.

Table 7.2.6 Front / Back Porch

FP3 BP3	FP2 BP2	FP1 BP1	FP0 BP0	# of Raster Periods In the Front Porch (2 Phase Gate Clock)	# of Raster Periods In the Front Porch (4 Phase Gate Clock)	# of Raster Periods In the Back Porch (4 Phase Gate Clock)	# of Raster Periods In the Back Porch (2 Phase Gate Clock)
0	0	0	0	Setting Disabled	Setting Disabled	Setting Disabled	Setting Disabled
0	0	0	1	1	Setting Disabled	Setting Disabled	Setting Disabled
0	0	1	0	2	2	2	Setting Disabled
0	0	1	1	3	3	3	3
0	1	0	0	4	4	4	4
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	0	0	12	12	12	12
1	1	0	1	13	13	13	13
1	1	1	0	14	14	14	14
1	1	1	1	Setting Disabled	Setting Disabled	Setting Disabled	Setting Disabled

NOTE: In the interlace drive mode, FP and BP setting is ignored: total sum of blanking period between 2 frames is automatically set to be 12 raster-rows. In the case of internal display mode, FP and BP settings are automatically set to be 8 raster-rows.

In RGB and VSYNC mode, BP + FP value must be even.

Frame Cycle Control 1 (R0AH):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	0	0	0	0	ECS 3	ECS 2	ECS 1	ECS 0	0	0	0	RTN 4	RTN 3	RTN 2	RTN 1	RTN 0
default	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1

ECS: ECS period is sustained for the number of clock cycle which is set on ECS 3-0.

ECS3	ECS2	ECS1	ECS0	ECS period		
				Internal Operation (synchronized with internal clock)	RGB I/F Operation (synchronized with DOTCLK)	
					18-/16-Bit	6-Bit
0	0	0	0	0	0	0
0	0	0	1	1 clock cycle	4 clock cycle	12 clock cycle
0	0	1	0	2 clock cycle	8 clock cycle	24 clock cycle
0	0	1	1	3 clock cycle	12 clock cycle	36 clock cycle
0	1	0	0	4 clock cycle	16 clock cycle	32 clock cycle
0	1	0	1	5 clock cycle	20 clock cycle	60 clock cycle
0	1	1	0	6 clock cycle	24 clock cycle	72 clock cycle
0	1	1	1	7 clock cycle	28 clock cycle	84 clock cycle
1	0	0	0	8 clock cycle	32 clock cycle	96 clock cycle
1	0	0	1	9 clock cycle	36 clock cycle	108 clock cycle
1	0	1	0	10 clock cycle	40 clock cycle	120 clock cycle
1	0	1	1	11 clock cycle	44 clock cycle	132 clock cycle
1	1	0	0	12 clock cycle	48 clock cycle	144 clock cycle
1	1	0	1	13 clock cycle	52 clock cycle	156 clock cycle
1	1	1	0	14 clock cycle	56 clock cycle	168 clock cycle
1	1	1	1	15 clock cycle	60 clock cycle	180 clock cycle

NOTE : ECS period must be less than R_STP value.

RTN4-0: Set the 1H period (1 raster-row).

RTN4	RTN3	RTN2	RTN1	RTN0	Horizontal clock frequency (CL1)	Clock frequency for step-up circuits (DCCLK)
0	0	0	0	0	32 clock cycle	fosc / 16
0	0	0	0	1	33 clock cycle	
0	0	0	1	0	34 clock cycle	fosc / 17
0	0	0	1	1	35 clock cycle	
0	0	1	0	0	36 clock cycle	fosc / 18
0	0	1	0	1	37 clock cycle	
0	0	1	1	0	38 clock cycle	fosc / 19
0	0	1	1	1	39 clock cycle	
0	1	0	0	0	40 clock cycle	fosc / 20
0	1	0	0	1	41 clock cycle	
0	1	0	1	0	42 clock cycle	fosc / 21
0	1	0	1	1	43 clock cycle	
0	1	1	0	0	44 clock cycle	fosc / 22
0	1	1	0	1	45 clock cycle	
0	1	1	1	0	46 clock cycle	fosc / 23
0	1	1	1	1	47 clock cycle	
1	0	0	0	0	48 clock cycle	fosc / 24
1	0	0	0	1	49 clock cycle	
1	0	0	1	0	50 clock cycle	fosc / 25
1	0	0	1	1	51 clock cycle	
1	0	1	0	0	52 clock cycle	fosc / 26
1	0	1	0	1	53 clock cycle	
1	0	1	1	0	54 clock cycle	fosc / 27
1	0	1	1	1	55 clock cycle	
1	1	0	0	0	56 clock cycle	fosc / 28
1	1	0	0	1	57 clock cycle	
1	1	0	1	0	58 clock cycle	fosc / 29
1	1	0	1	1	59 clock cycle	
1	1	1	0	0	60 clock cycle	fosc / 30
1	1	1	0	1	61 clock cycle	
1	1	1	1	0	62 clock cycle	fosc / 31
1	1	1	1	1	63 clock cycle	

Frame Cycle Control 2 (R0BH):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DCR 2	DCR 1	DCR 0
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

DCR 2-0: Set clock cycle for step-up circuit in external interface mode. Please set DM bit to “10” and DCR2-0 value when external interface is in use. In this case, DOTCLK must be input periodically and continuously.

The external clock is the DCCLK (clock cycle for step-up circuit) source, when external interface mode is in use (DM =”10”).

DCR2	DCR1	DCR0	Clock cycle for step-up circuits (DCCLK) in external interface mode	
			18-/16-Bit	6-Bit
0	0	0	DOTCLK/64	DOTCLK/192
0	0	1	DOTCLK/96	DOTCLK/288
0	1	0	DOTCLK/112	DOTCLK/336
0	1	1	DOTCLK/128	DOTCLK/384
1	0	0	DOTCLK/144	DOTCLK/432
1	0	1	DOTCLK/160	DOTCLK/480
1	1	0	DOTCLK/192	DOTCLK/576
1	1	1	DOTCLK/224	DOTCLK/672

NOTE: If external input clock cycle is variable or discontinuous, clock cycle for step-up circuit must be generated internally (RM=0).

External Interface Control (R0CH):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	0	0	0	0	0	0	0	0	0	RM	DM1	DM0	0	0	RIM1	RIM0
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RM: Specifies the interface for RAM accesses. When the display data is written via the RGB interface, RM bit should be set (RM = 1). This bit and the DM bits can be set independently. The display data can be written via the system interface by clearing this bit while the RGB interface is used.

RM	Interface for RAM Access
0	System interface / VSYNC interface
1	RGB interface

NOTE: "RM=0 & DM =01" is not supported.

DM1-0: Specify the display operation mode. The interface operation is based on the bits of DM1-0. This setting enables switching interface between internal operation and the external display interface. Switching among two external display interfaces (RGB and VSYNC interface) should not be done. The external clock is the DCCLK (clock cycle for step-up circuit) source, when external interface mode is in use (DM ="01").

DM1	DM0	Display Operation Mode	Display Operation Mode in MDDI
0	0	Internal clock operation	Internal clock operation
0	1	RGB interface	disable
1	0	VSYNC interface	VSYNC interface
1	1	Setting prohibit	Setting prohibit

NOTE: In case of "RM=0 and DM =01", must be write 1 frame image data to GRAM in 1 frame before.

RIM1-0: Specify the RGB interface mode when the RGB interface is used. Specifically, this setting specifies the mode when the bits of DM and RM are set to RGB interface. These bits should be set before display operation through the RGB interface and should not be set during operation.

RIM1	RIM0	RGB Interface Mode
0	0	18-bit RGB interface (one transfer/pixel)
0	1	16-bit RGB interface (one transfer /pixel)
1	0	6-bit RGB interface (three transfers /pixel)
1	1	Setting disable / prohibit

Depending on the external display interface setting, various interfaces can be specified to match the display state. While displaying motion picture on the RGB interface, the data for display can be written in high-speed write mode. This method can achieve both low power consumption and high-speed access.

Table 7.2.7 Display State and Interface

Display State	Operation Mode	RAM Access (RM)	Display Operation Mode (DM)
Still Pictures or Motion Picture Display	Internal Clock	System interface (RM=0)	Internal clock (DM=00)
Motion Picture Display	RGB interface	RGB interface (RM=1)	RGB interface (DM=01)
Motion Picture Display	VSYNC interface	System interface (RM=0)	VSYNC interface (DM1-0=10)

NOTES: 1) The instruction register can only be set through the system interface.
2) RGB interface modes should not be set during operation.
3) For the transition flow for each operation mode, see the External Display Interface section.

Power Control 1 (R10H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SLP	STB
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SLP: When SLP is high, the S6D1121 enters the sleep mode. The internal display operations are halted except for the R-C oscillator for reducing current consumption. Only the following instructions except of some commands (*note) can be executed during the sleep mode. During the sleep mode, the other GRAM data do not updated. Register set-up is maintained.

NOTE: Some commands which are D1, D0, and GON

STB: When STB is high, the S6D1121 enters the standby mode, where display operation completely stops. This mode can halt all the internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied. For details, see the Standby Mode section.

Level	Condition
VCOM	AVSS
LTPS (Gate Clock / RGB Multiplexer Clock)	VGH
Source	AVSS

Power Control 2 (R11H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	0	0	VRH 5	VRH 4	VRH 3	VRH 2	VRH 1	VRH 0	0	0	VCI1 _OFF	0	0	VC2	VC1	VC0
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

VRH5-0: Set the amplified factor of the GVDD voltage (the voltage for the Gamma voltage). It allows amplify from 3.0v to 5.0v

VRH5	VRH4	VRH3	VRH2	VRH1	VRH0	GVDD	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0	GVDD
0	0	0	0	0	0	3.00V	1	0	0	0	0	0	4.01V
0	0	0	0	0	1	3.03V	1	0	0	0	0	1	4.05V
0	0	0	0	1	0	3.06V	1	0	0	0	1	0	4.08V
0	0	0	0	1	1	3.09V	1	0	0	0	1	1	4.11V
0	0	0	1	0	0	3.12V	1	0	0	1	0	0	4.14V
0	0	0	1	0	1	3.16V	1	0	0	1	0	1	4.17V
0	0	0	1	1	0	3.19V	1	0	0	1	1	0	4.21V
0	0	0	1	1	1	3.22V	1	0	0	1	1	1	4.24V
0	0	1	0	0	0	3.25V	1	0	1	0	0	0	4.27V
0	0	1	0	0	1	3.28V	1	0	1	0	0	1	4.30V
0	0	1	0	1	0	3.31V	1	0	1	0	1	0	4.33V
0	0	1	0	1	1	3.35V	1	0	1	0	1	1	4.36V
0	0	1	1	0	0	3.38V	1	0	1	1	0	0	4.40V
0	0	1	1	0	1	3.41V	1	0	1	1	0	1	4.43V
0	0	1	1	1	0	3.44V	1	0	1	1	1	0	4.46V
0	0	1	1	1	1	3.47V	1	0	1	1	1	1	4.49V
0	1	0	0	0	0	3.51V	1	1	0	0	0	0	4.52V
0	1	0	0	0	1	3.54V	1	1	0	0	0	1	4.56V
0	1	0	0	1	0	3.57V	1	1	0	0	1	0	4.59V
0	1	0	0	1	1	3.60V	1	1	0	0	1	1	4.62V
0	1	0	1	0	0	3.63V	1	1	0	1	0	0	4.65V
0	1	0	1	0	1	3.66V	1	1	0	1	0	1	4.68V
0	1	0	1	1	0	3.70V	1	1	0	1	1	0	4.71V
0	1	0	1	1	1	3.73V	1	1	0	1	1	1	4.75V
0	1	1	0	0	0	3.76V	1	1	1	0	0	0	4.78V
0	1	1	0	0	1	3.79V	1	1	1	0	0	1	4.81V
0	1	1	0	1	0	3.82V	1	1	1	0	1	0	4.84V
0	1	1	0	1	1	3.86V	1	1	1	0	1	1	4.87V
0	1	1	1	0	0	3.89V	1	1	1	1	0	0	4.91V
0	1	1	1	0	1	3.92V	1	1	1	1	0	1	4.94V
0	1	1	1	1	0	3.95V	1	1	1	1	1	0	4.97V
0	1	1	1	1	1	3.98V	1	1	1	1	1	1	5.00V

VCI1_OFF: VCI1 amp off register. If VCI1_OFF = H, VCI1 pad and VCI pad external short

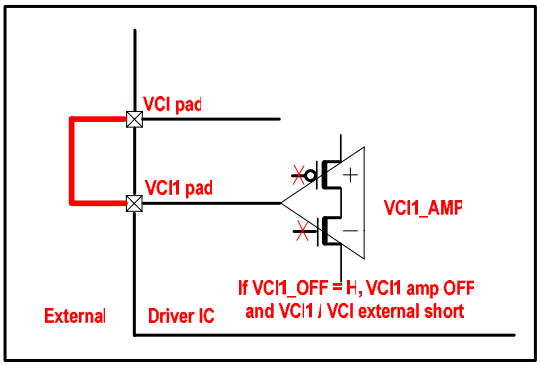


Figure 7.2.5 The circuit for VCI1_OFF funcion

VC2-0: Set the VCI1 voltage. These bits set the VCI1 voltage from 0.68 to 1 times of the VCI_REF voltage.VCI1 is AVDD reference voltage.

VC2	VC1	VC0	VCI1
0	0	0	0.68 X VCI_REF
0	0	1	0.83 X VCI_REF
0	1	0	0.92 X VCI_REF
0	1	1	1.00 X VCI_REF
1	0	0	0.575 X VCI_REF

NOTE: Don't set any higher VCI1 level than 3.0V

Power Control 3 (R12H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	0	0	0	0	0	0	0	0	0	SAP 2	SAP 1	SAP 0	0	DC2	DC1	DC0
default	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1

SAP2-0: Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver. When the amount of fixed current is large, LCD driving ability and the display quality become high, but the current consumption is increased. Adjust the fixed current considering the display quality and the current consumption. During non-display, when SAP2-0 = “000”, the current consumption can be reduced by ending the operational amplifier and step-up circuit operation.

SAP2	SAP1	SAP0	Amount of Current in Operational Amplifier
0	0	0	Source amp halt
0	0	1	Low
0	1	0	Medium Low
0	1	1	Medium
1	0	0	Medium High
1	0	1	Large
1	1	0	Medium Large
1	1	1	Largest

DC2-0: The operating frequency in the step-up circuit is selected. When the step-up operating frequency is high, the driving ability of the step-up circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.

DC2	DC1	DC0	Step-up Cycle in Step-up Circuit 1,3	Step-up Cycle in Step-up Circuit 2
0	0	0	DCCLK / 1	DCCLK / 1
0	0	1	DCCLK / 1	DCCLK / 2
0	1	0	DCCLK / 1	DCCLK / 4
0	1	1	DCCLK / 2	DCCLK / 2
1	0	0	DCCLK / 2	DCCLK / 4
1	0	1	DCCLK / 4	DCCLK / 4
1	1	0	DCCLK / 4	DCCLK / 8
1	1	1	DCCLK / 4	DCCLK / 16

NOTE: DCCLK is Clock frequency for step-up circuits

Power Control 4 (R13H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	VR2 C3	VR2 C2	VR2 C1	VR2 C0	VR1 C3	VR1 C2	VR1 C1	VR1 C0	VGL RC4	VGL RC3	VGL RC2	VGL RC1	VGL RC0	PON	PON1	AON
default	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

VR1C3-0: Set the VR1 voltage. These bits set the VR1 voltage from 2.0 to 5.0. VR1 voltage is VGH, VGL reference voltage.

VR2C3-0: Set the VR2 voltage. These bits set the VR2 voltage from 2.0 to 5.0. VR2 voltage is VGH reference voltage.

VR1C3	VR1C2	VR1C1	VR1C0	VR1	VR2C3	VR2C2	VR2C1	VR2C0	VR2
0	0	0	0	2.00	0	0	0	0	2.00
0	0	0	1	2.25	0	0	0	1	2.25
0	0	1	0	2.50	0	0	1	0	2.50
0	0	1	1	2.75	0	0	1	1	2.75
0	1	0	0	3.00	0	1	0	0	3.00
0	1	0	1	3.25	0	1	0	1	3.25
0	1	1	0	3.50	0	1	1	0	3.50
0	1	1	1	3.75	0	1	1	1	3.75
1	0	0	0	4.00	1	0	0	0	4.00
1	0	0	1	4.25	1	0	0	1	4.25
1	0	1	0	4.50	1	0	1	0	4.50
1	0	1	1	4.75	1	0	1	1	4.75
1	1	0	0	5.00	1	1	0	0	5.00

VGH: VGH voltage is gate positive voltage. VGH is generated by AVDD + VR1 + VR2.VGH range is 7.5 ~ 16.0V

VGL: VGL voltage is VGLROUT regulator power voltage. VGL is generated by –(AVDD + VR1). VGL range is –11.0 ~ 5.5V

VGLROUT: VGLROUT voltage is gate negative voltage. VGLROUT is generated by regulator amp. VGLRC register is VGLROUT level control. VGLROUT range is –10.5 ~ -5.0V

VGLRC4-0: Set the VGLROUT voltage. These bits set the VGLROUT voltage from –10.5 to -5.0. VGLROUT voltage is gate negative voltage.

VGLRC4	VGLRC3	VGLRC2	VGLRC1	VGLRC0	VGLROUT
0	0	0	0	0	-4.988
0	0	0	0	1	-5.250
0	0	0	1	0	-5.513
0	0	0	1	1	-5.775
0	0	1	0	0	-6.038
0	0	1	0	1	-6.300
0	0	1	1	0	-6.563
0	0	1	1	1	-6.825
0	1	0	0	0	-7.088
0	1	0	0	1	-7.350
0	1	0	1	0	-7.613
0	1	0	1	1	-7.875
0	1	1	0	0	-8.138
0	1	1	0	1	-8.400
0	1	1	1	0	-8.663
0	1	1	1	1	-8.925
1	0	0	0	0	-9.188
1	0	0	0	1	-9.450
1	0	0	1	0	-9.713
1	0	0	1	1	-9.975
1	0	1	0	0	-10.238
1	0	1	0	1	-10.500

PON: This is an operation-starting bit for the booster circuit1. In case of PON = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the PON = 1, please refer to the SET UP FLOW OF POWER SUPPLY.

PON1: This is an operation-starting bit for the booster circuit 2. In case of PON1 = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the PON1= 1, please refer to the SET UP FLOW OF POWER SUPPLY.

AON: This is an operation-starting bit for the Amplifier. In case of AON = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the AON= 1, please refer to the SET UP FLOW OF POWER SUPPLY.

Power Control 5 (R14H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	0	0	VCM 5	VCM 4	VCM 3	VCM 2	VCM 1	VCM 0	0	0	VML 5	VML 4	VML 3	VML 2	VML 1	VML 0
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VCM5-0: Set the VCOMDC voltage. Voltage range is from 2.4 volt to 4.0 volt. Using this command in case of coupling driving method.

(Vref = 2.0V)

VCM 5	VCM 4	VCM 3	VCM 2	VCM 1	VCM 0	VCOMDC Voltage	VCM 5	VCM 4	VCM 3	VCM 2	VCM 1	VCM 0	VCOMDC Voltage
0	0	0	0	0	0	2.40 V	1	0	0	0	0	0	3.21 V
0	0	0	0	0	1	2.43 V	1	0	0	0	0	1	3.24 V
0	0	0	0	1	0	2.45 V	1	0	0	0	1	0	3.26 V
0	0	0	0	1	1	2.48 V	1	0	0	0	1	1	3.29 V
0	0	0	1	0	0	2.50 V	1	0	0	1	0	0	3.31 V
0	0	0	1	0	1	2.53 V	1	0	0	1	0	1	3.34 V
0	0	0	1	1	0	2.55 V	1	0	0	1	1	0	3.37 V
0	0	0	1	1	1	2.58 V	1	0	0	1	1	1	3.39 V
0	0	1	0	0	0	2.60 V	1	0	1	0	0	0	3.42 V
0	0	1	0	0	1	2.63 V	1	0	1	0	0	1	3.44 V
0	0	1	0	1	0	2.65 V	1	0	1	0	1	0	3.47 V
0	0	1	0	1	1	2.68 V	1	0	1	0	1	1	3.49 V
0	0	1	1	0	0	2.70 V	1	0	1	1	0	0	3.52 V
0	0	1	1	0	1	2.73 V	1	0	1	1	0	1	3.54 V
0	0	1	1	1	0	2.76 V	1	0	1	1	1	0	3.57 V
0	0	1	1	1	1	2.78 V	1	0	1	1	1	1	3.59 V
0	1	0	0	0	0	2.81 V	1	1	0	0	0	0	3.62 V
0	1	0	0	0	1	2.83 V	1	1	0	0	0	1	3.64 V
0	1	0	0	1	0	2.86 V	1	1	0	0	1	0	3.67 V
0	1	0	0	1	1	2.88 V	1	1	0	0	1	1	3.70 V
0	1	0	1	0	0	2.91 V	1	1	0	1	0	0	3.72 V
0	1	0	1	0	1	2.93 V	1	1	0	1	0	1	3.75 V
0	1	0	1	1	0	2.96 V	1	1	0	1	1	0	3.77 V
0	1	0	1	1	1	2.98 V	1	1	0	1	1	1	3.80 V
0	1	1	0	0	0	3.01 V	1	1	1	0	0	0	3.82 V
0	1	1	0	0	1	3.03 V	1	1	1	0	0	1	3.85 V
0	1	1	0	1	0	3.06 V	1	1	1	0	1	0	3.87 V
0	1	1	0	1	1	3.09 V	1	1	1	0	1	1	3.90 V
0	1	1	1	0	0	3.11 V	1	1	1	1	0	0	3.92 V
0	1	1	1	0	1	3.14 V	1	1	1	1	0	1	3.95 V
0	1	1	1	1	0	3.16 V	1	1	1	1	1	0	3.97 V
0	1	1	1	1	1	3.19 V	1	1	1	1	1	1	4.00V

NOTE: Set VCOMDC range from 2.4V to 4.0V. (In the case of Vref=2.0V)

VML5-0: Set the VCOML voltage. Voltage range is from 0 volt to 1.0 volt.

(Vref = 2.0V)

VML 5	VML 4	VML 3	VML 2	VML 1	VML 0	Amplitude of Voltage	VML 5	VML 4	VML 3	VML 2	VML 1	VML 0	Amplitude of Voltage
0	0	0	0	0	0	2.52 V	1	0	0	0	0	0	3.75 V
0	0	0	0	0	1	2.56 V	1	0	0	0	0	1	3.78 V
0	0	0	0	1	0	2.60 V	1	0	0	0	1	0	3.82 V
0	0	0	0	1	1	2.64 V	1	0	0	0	1	1	3.86 V
0	0	0	1	0	0	2.68 V	1	0	0	1	0	0	3.90 V
0	0	0	1	0	1	2.71 V	1	0	0	1	0	1	3.94 V
0	0	0	1	1	0	2.75 V	1	0	0	1	1	0	3.97 V
0	0	0	1	1	1	2.79 V	1	0	0	1	1	1	4.01 V
0	0	1	0	0	0	2.83 V	1	0	1	0	0	0	4.05 V
0	0	1	0	0	1	2.87 V	1	0	1	0	0	1	4.09 V
0	0	1	0	1	0	2.90 V	1	0	1	0	1	0	4.13 V
0	0	1	0	1	1	2.94 V	1	0	1	0	1	1	4.17 V
0	0	1	1	0	0	2.98 V	1	0	1	1	0	0	4.20 V
0	0	1	1	0	1	3.02 V	1	0	1	1	0	1	4.24 V
0	0	1	1	1	0	3.06 V	1	0	1	1	1	0	4.28 V
0	0	1	1	1	1	3.10 V	1	0	1	1	1	1	4.32 V
0	1	0	0	0	0	3.13 V	1	1	0	0	0	0	4.36 V
0	1	0	0	0	1	3.17 V	1	1	0	0	0	1	4.39 V
0	1	0	0	1	0	3.21 V	1	1	0	0	1	0	4.43 V
0	1	0	0	1	1	3.25 V	1	1	0	0	1	1	4.47 V
0	1	0	1	0	0	3.29 V	1	1	0	1	0	0	4.51 V
0	1	0	1	0	1	3.32 V	1	1	0	1	0	1	4.55 V
0	1	0	1	1	0	3.36 V	1	1	0	1	1	0	4.62 V
0	1	0	1	1	1	3.40 V	1	1	0	1	1	1	4.70 V
0	1	1	0	0	0	3.44 V	1	1	1	0	0	0	4.78 V
0	1	1	0	0	1	3.48 V	1	1	1	0	0	1	4.85 V
0	1	1	0	1	0	3.52 V	1	1	1	0	1	0	4.93 V
0	1	1	0	1	1	3.55 V	1	1	1	0	1	1	5.01 V
0	1	1	1	0	0	3.59 V	1	1	1	1	0	0	5.08 V
0	1	1	1	0	1	3.63 V	1	1	1	1	0	1	5.16 V
0	1	1	1	1	0	3.67 V	1	1	1	1	1	0	5.24 V
0	1	1	1	1	1	3.71 V	1	1	1	1	1	1	5.31 V

NOTE: Set VCOML range from 0V to 1.0V. (In the case of Vref=2.0V)

Power Control 6 (R15H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	VCMR	0	VMA5	VMA4	VMA3	VMA2	VMA1	VMA0	0	0	VMH5	VMH4	VMH3	VMH2	VMH1	VMH0
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VCMR: If VCMR is LOW and direct driving method for VCOM generation, VCOMH is adjusted by VMA5-0 Register and VCOMR pin is used to monitor the input voltage of the AMP which outputs the VCOMH voltage. And, if VCMR is LOW and coupling driving method for VCOM generation, VCOMH is adjusted by VMA5-0 Register and VCOMR pin is used to monitor the input voltage of the AMP which outputs the VCOMH voltage.

If VCMR is HIGH and direct driving method for VCOM generation, VMA5-0 register is ignored and VCOMH voltage is adjusted by external VCOMR voltage. And, if VCMR is HIGH and coupling driving method for VCOM generation, VMA5-0 register is ignored and VCOMH voltage is adjusted by external VCOMR voltage. The relationship between VCOMH and VCOMR is given as VCOMH=2.65 x VCOMR. VCOMR range is 1.328V ~ 2.0V

VMA5-0: Set the VCOMH voltage. Voltage range is from 3.52 volt to 5.30 volt.

(Vref = 2.0V)

VMA5	VMA4	VMA3	VMA2	VMA1	VMA0	VCOMH Voltage	VMA5	VMA4	VMA3	VMA2	VMA1	VMA0	VCOMH Voltage
0	0	0	0	0	0	Prohibit	1	0	0	0	0	0	4.26 V
0	0	0	0	0	1	Prohibit	1	0	0	0	0	1	4.29 V
0	0	0	0	1	0	Prohibit	1	0	0	0	1	0	4.32 V
0	0	0	0	1	1	Prohibit	1	0	0	0	1	1	4.36 V
0	0	0	1	0	0	Prohibit	1	0	0	1	0	0	4.39 V
0	0	0	1	0	1	Prohibit	1	0	0	1	0	1	4.43 V
0	0	0	1	1	0	Prohibit	1	0	0	1	1	0	4.46 V
0	0	0	1	1	1	Prohibit	1	0	0	1	1	1	4.49 V
0	0	1	0	0	0	Prohibit	1	0	1	0	0	0	4.53 V
0	0	1	0	0	1	Prohibit	1	0	1	0	0	1	4.56 V
0	0	1	0	1	0	3.52 V	1	0	1	0	1	0	4.59 V
0	0	1	0	1	1	3.55 V	1	0	1	0	1	1	4.63 V
0	0	1	1	0	0	3.58 V	1	0	1	1	0	0	4.66 V
0	0	1	1	0	1	3.62 V	1	0	1	1	0	1	4.69 V
0	0	1	1	1	0	3.65 V	1	0	1	1	1	0	4.73 V
0	0	1	1	1	1	3.68 V	1	0	1	1	1	1	4.76 V
0	1	0	0	0	0	3.72 V	1	1	0	0	0	0	4.80 V
0	1	0	0	0	1	3.75 V	1	1	0	0	0	1	4.83 V
0	1	0	0	1	0	3.79 V	1	1	0	0	1	0	4.86 V
0	1	0	0	1	1	3.82 V	1	1	0	0	1	1	4.90 V
0	1	0	1	0	0	3.85 V	1	1	0	1	0	0	4.93 V
0	1	0	1	0	1	3.89 V	1	1	0	1	0	1	4.96 V
0	1	0	1	1	0	3.92 V	1	1	0	1	1	0	5.00 V
0	1	0	1	1	1	3.95 V	1	1	0	1	1	1	5.03 V
0	1	1	0	0	0	3.99 V	1	1	1	0	0	0	5.06 V
0	1	1	0	0	1	4.02 V	1	1	1	0	0	1	5.10 V
0	1	1	0	1	0	4.05 V	1	1	1	0	1	0	5.13 V
0	1	1	0	1	1	4.09 V	1	1	1	0	1	1	5.17 V
0	1	1	1	0	0	4.12 V	1	1	1	1	0	0	5.20 V
0	1	1	1	0	1	4.16 V	1	1	1	1	0	1	5.23 V
0	1	1	1	1	0	4.19 V	1	1	1	1	1	0	5.27 V
0	1	1	1	1	1	4.22 V	1	1	1	1	1	1	5.30 V

NOTE: Set VCOMH range from 3.52V to 5.3V. (In the case of Vref=2.0V)

VMH5-0: Set the VCOMPREC voltage. Voltage range is from 3.60 volt to 6.00 volt.

(Vref = 2.0V)

VMH 5	VMH 4	VMH 3	VMH 2	VMH 1	VMH 0	VCOMPREC Voltage	VMH 5	VMH 4	VMH 3	VMH 2	VMH 1	VMH 0	VCOMPREC Voltage
0	0	0	0	0	0	3.60 V	1	0	0	0	0	0	4.82 V
0	0	0	0	0	1	3.64 V	1	0	0	0	0	1	4.86 V
0	0	0	0	1	0	3.68 V	1	0	0	0	1	0	4.90 V
0	0	0	0	1	1	3.71 V	1	0	0	0	1	1	4.93 V
0	0	0	1	0	0	3.75 V	1	0	0	1	0	0	4.97 V
0	0	0	1	0	1	3.79 V	1	0	0	1	0	1	5.01 V
0	0	0	1	1	0	3.83 V	1	0	0	1	1	0	5.05 V
0	0	0	1	1	1	3.87 V	1	0	0	1	1	1	5.09 V
0	0	1	0	0	0	3.90 V	1	0	1	0	0	0	5.12 V
0	0	1	0	0	1	3.94 V	1	0	1	0	0	1	5.16 V
0	0	1	0	1	0	3.98 V	1	0	1	0	1	0	5.20 V
0	0	1	0	1	1	4.02 V	1	0	1	0	1	1	5.24 V
0	0	1	1	0	0	4.06 V	1	0	1	1	0	0	5.28 V
0	0	1	1	0	1	4.10 V	1	0	1	1	0	1	5.31 V
0	0	1	1	1	0	4.13 V	1	0	1	1	1	0	5.35 V
0	0	1	1	1	1	4.17 V	1	0	1	1	1	1	5.39 V
0	1	0	0	0	0	4.21 V	1	1	0	0	0	0	5.43 V
0	1	0	0	0	1	4.25 V	1	1	0	0	0	1	5.47 V
0	1	0	0	1	0	4.29 V	1	1	0	0	1	0	5.50 V
0	1	0	0	1	1	4.32 V	1	1	0	0	1	1	5.54 V
0	1	0	1	0	0	4.36 V	1	1	0	1	0	0	5.58 V
0	1	0	1	0	1	4.40 V	1	1	0	1	0	1	5.62 V
0	1	0	1	1	0	4.44 V	1	1	0	1	1	0	5.66 V
0	1	0	1	1	1	4.48 V	1	1	0	1	1	1	5.70 V
0	1	1	0	0	0	4.51 V	1	1	1	0	0	0	5.73 V
0	1	1	0	0	1	4.55 V	1	1	1	0	0	1	5.77 V
0	1	1	0	1	0	4.59 V	1	1	1	0	1	0	5.81 V
0	1	1	0	1	1	4.63 V	1	1	1	0	1	1	5.85 V
0	1	1	1	0	0	4.67 V	1	1	1	1	0	0	5.89 V
0	1	1	1	0	1	4.70 V	1	1	1	1	0	1	5.92 V
0	1	1	1	1	0	4.74 V	1	1	1	1	1	0	5.96 V
0	1	1	1	1	1	4.78 V	1	1	1	1	1	1	6.00 V

NOTE: Set VCOMPREC range from 3.6V to 6.0V. (In the case of Vref=2.0V)

Power Control 7 (R16H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	0	0	0	0	0	0	0	0	VCOM_OFF	0	0	0	0	PREC	COMS	COMA
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

VCOM_OFF: control on / off of the VCOM, VCOMPREC and VCOMDC in the 2 phase gate clock mode.

PREC: control the pre-charge signal for VCOM.

COMS: selection signal for VCOM driving method (direct or coupling).

1: direct VCOM driving method

0: coupling VCOM driving method

COMA: setup VCOML voltage.

1: VCOML = 0V ~1V(control VML[5:0])

0: VCOML = AVSS

Table 7.2.8 Functional Table of Direct VCOM Driving and Coupling VCOM Driving Method

COMS	COMA	Functions
1	1	Using direct VCOM driving type, VcomL level is an output of OP amplifier.
	0	Using direct VCOM driving type and VcomL level is AVSS.
0	1	Using coupling VCOM driving type, VcomL level is an output of OP amplifier.
	0	Using coupling VCOM driving type and VcomL level is AVSS.

NOTES: When the setting value of FLD = 00 (2 phase gate clock driving mode) is “0”, the output signals relating VCOM are useless.

Table 7.2.9 Function Configuration Table of Direct VCOM Driving and Coupling VCOM Driving Method

COMS	COMA	FLD[1:0]	VCOM	VCOMPREC	VCOMDC
1	1	00	AVSS	AVSS	AVSS
		01,10,11	VcomH to VcomL	AVSS	AVSS
	0	00	AVSS	AVSS	AVSS
		01,10,11	VcomH to AVSS	AVSS	AVSS
0	1	00	AVSS	AVSS	AVSS
		01,10,11	VcomH to VcomL	After VMH setting value during PREC period, this value is floating.	VCM setting value
	0	00	AVSS	AVSS	AVSS
		01,10,11	VcomH to AVSS	After VMH setting value during PREC period, this value is floating.	VCM setting value

NOTES: When the setting value of FLD = 00 (2 phase gate clock driving mode), Panel is not use the VCOM, VCOMPREC, and VCOMDC.

RAM Address Set (R20H / R21H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W	0	0	0	0	0	0	0	0	AD 16	AD 15	AD 14	AD 13	AD 12	AD 11	AD 10	AD9	AD8
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AD16–0: Initially set GRAM addresses to the address counter (AC). Once the GRAM data is written, the AC is automatically updated according to I/D bit settings. This allows consecutive accesses without resetting address. Once the GRAM data is read, the AC is not automatically updated. GRAM address setting is not allowed in the standby mode. Ensure that the address is set within the specified window address. When RGB interface is in use (RM1-0=10), AD16-0 will be set at the falling edge of the VSYNC signal. When the internal clock operation and VSYNC interface (RM=0X) are in use, AD16-0 will be set upon execution of an instruction.

AD16 to AD0	GRAM setting
“00000”H to “000EF”H	Bitmap data for G1
“00100”H to “001EF”H	Bitmap data for G2
“00200”H to “002EF”H	Bitmap data for G3
“00300”H to “003EF”H	Bitmap data for G4
: : :	: : :
“13C00”H to “13CEF”H	Bitmap data for G317
“13D00”H to “13DEF”H	Bitmap data for G318
“13E00”H to “13EEF”H	Bitmap data for G319
“13F00”H to “13FEF”H	Bitmap data for G320

Read / Write Data to GRAM (R22H):

GRAM WRITE DATA:

R/W	RS	IB17	IB16	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	WDR [17:0] (Bit assignment from DB or PD to WD varies with interface mode.)																	

WDR [17:0]: Input data for GRAM can be expanded to 18 bits. The expansion format varies according to the interface method. The input data selects the grayscale level. After a write, the address is automatically updated according to AM and I/D bit settings. The GRAM cannot be accessed in standby mode. When 16- or 8-bit interface is in use, the write data is expanded to 18 bits by writing the MSB of the <R><B> data to its LSB.

When written data to GRAM is used by RGB interface via the system interface, please make sure that writing data do not cause conflicts.

When the 18-bit RGB interface is in use, 18-bit data is written to RAM via PD17-0. This interface is available on the 262,144-colors. When the 16-bit RGB interface is in use, the MSB is written to its LSB. This interface is available on the 65,536-colors.

GRAM READ DATA:

R/W	RS	IB17	IB16	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	RDR [17:0] (Bit assignment from RD to DB varies with interface mode.)																	

RDR [17:0]: Read 18-bit data from the GRAM. When the data is read to the MCU, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (DB15–0) becomes invalid and the second-word read is normal.

GAMMA Control 1 ~12 (R30H ~ R3BH):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R/W	1	0	0	PKP1 [5:0]						0	0	PKP0 [5:0]					
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	1	0	0	PKP3 [5:0]						0	0	PKP2 [5:0]					
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	1	0	0	PKP5 [5:0]						0	0	PKP4 [5:0]					
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	1	0	0	PKP7 [5:0]						0	0	PKP6 [5:0]					
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	1	0	0	PKP9 [5:0]						0	0	PKP8 [5:0]					
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	1	0	0	PKP11 [5:0]						0	0	PKP10 [5:0]					
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	1	0	0	PKN1 [5:0]						0	0	PKN0 [5:0]					
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	1	0	0	PKN3 [5:0]						0	0	PKN2 [5:0]					
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	1	0	0	PKN5 [5:0]						0	0	PKN4 [5:0]					
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	1	0	0	PKN7 [5:0]						0	0	PKN6 [5:0]					
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	1	0	0	PKN9 [5:0]						0	0	PKN8 [5:0]					
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	1	0	0	PKN11 [5:0]						0	0	PKN10 [5:0]					
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	1	0	0	0	VRP1 [4:0]					0	0	0	VRP0 [4:0]				
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	1	0	0	0	VRN1 [4:0]					0	0	0	VRN0 [4:0]				
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PKP11 ~ 0 [5:0]: The gamma fine adjustment register for the positive polarity output

PKN11 ~ 0 [5:0]: The gamma fine adjustment register for the negative polarity output

VRP1 [4:0]: The amplitude adjustment register for the positive polarity output

VRN1 [4:0]: The amplitude adjustment register for the negative polarity output

VRP0 [4:0]: The reference adjustment register for the positive polarity output

VRN0 [4:0]: The reference adjustment register for the negative polarity output

For details, see the GAMMA ADJUSTMENT FUNCTION.

Vertical Scroll Control (R41H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VL8-0: Specify scroll length at the scroll display for vertical smooth scrolling. Any raster-row from the 1st to 320th can be scrolled according to the value of VL8-0. After 320th raster-row is displayed, the display restarts from the first raster-row. The scroll length (VL8-0) is valid when VLE1 = 1 or VLE2 = 1. The raster-row display is fixed when VLE2-1 = 00.

VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Scroll Length
0	0	0	0	0	0	0	0	0	0 raster-row
0	0	0	0	0	0	0	0	1	1 raster-row
0	0	0	0	0	0	0	1	0	2 raster-row
				.					.
				.					.
				.					.
1	0	0	1	1	1	1	1	0	318 raster-row
1	0	0	1	1	1	1	1	1	319 raster-row

NOTES:

1. Don't set any higher raster-row than 319 ("13F"H).
2. Also, make sure that the condition of below table (Table 7.2.9)

Table 7.2.10 VL Setting Value on the Vertical Scroll Operation

SPT	VLE[1:0]	VL Setting Value
0	X	SE1 – SS1 ≥ VL (operation of scroll area 1 field)
1	"01"	SE1 – SS1 ≥ VL (operation of scroll area 1 field)
	"10"	SE2 – SS2 ≥ VL (operation of scroll area 2 field)

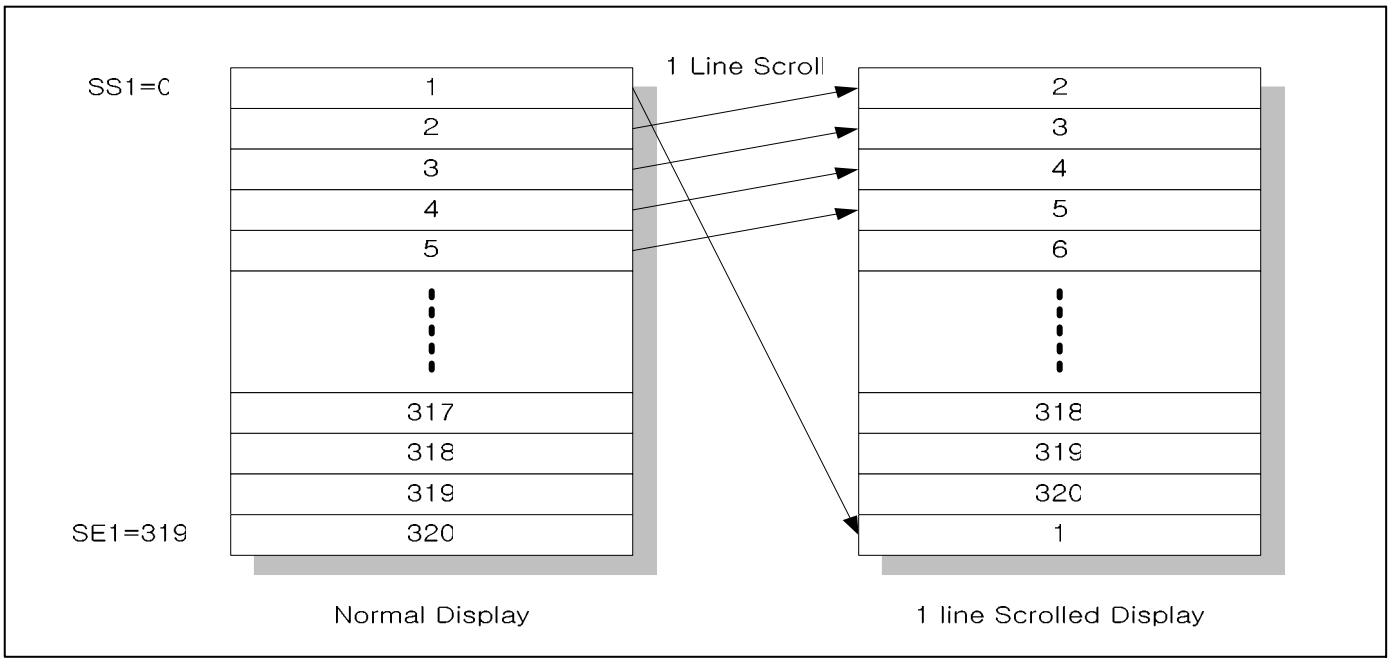


Figure 7.2.6 Scroll Function (SS1 = 0, SE1 = 319, VL = 1, SPT = 0)

1st Screen Driving Position (R42H / R43H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	SE18	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
default	1	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1
W	1	0	0	0	0	0	0	0	SS18	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
default	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

2nd Screen Driving Position (R44H / R45H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	SE28	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20
default	1	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1
W	1	0	0	0	0	0	0	0	SS28	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20
default	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SS18–10: Specify the driving starting position for the first screen in a line unit. The LCD driving starts from the ‘set value +1’ gate driver.

SE18–10: Specify the driving end position for the first screen in a line unit. The LCD driving is performed to the ‘set value + 1’ gate driver. For instance, when SS18–10 = 07h and SE18–10 = 10h are set, the LCD driving is performed from G8 to G17, and non-display driving is performed for G1 to G7, G18, and others. Ensure that SS18 to 10 ≤ SE18 to 10 ≤ 13Fh. For details, see the Screen-division Driving Function section.

SS28–20: Specify the driving start position for the second screen in a line unit. The LCD driving starts from the ‘set value + 1’ of the gate driver. The second screen is driven when SPT = 1.

SE28–20: Specify the driving end position for the second screen in a line unit. The LCD driving is performed to the ‘set value + 1’ of the gate driver. For instance, when SPT = 1, SS28–20 = 20h, and SE28–20 = 13Fh are set, the LCD driving is performed from G33 to G320. Ensure that SS18 to 10 ≤ SE18 to 10 < SS28 to 20 ≤ SE28 to 20 ≤ 13Fh. For details, see the Screen-division Driving Function section.

Horizontal Window Address Position (R46H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	HEA 7	HEA 6	HEA 5	HEA 4	HEA 3	HEA 2	HEA 1	HEA 0	HSA 7	HSA 6	HSA 5	HSA 4	HSA 3	HSA 2	HSA 1	HSA 0
default	1	1	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0

Vertical Window Address Position (R47H / R48H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	VEA 8	VEA 7	VEA 6	VEA 5	VEA 4	VEA 3	VEA 2	VEA 1	VEA 0
default	1	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1
W	1	0	0	0	0	0	0	0	VSA 8	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0
default	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

HSA7-0/HEA7-0: Specify the horizontal start/end positions of a window for access in memory. Data can be written to the GRAM. The written data is from the address specified by HSA7-0 to the address specified by HEA 7-0. Note that an address must be set before RAM data are written. Ensure 00h ≤ HSA7-0 ≤ HEA7-0 ≤ Efh.

VSA8-0/VEA8-0: Specify the vertical start/end positions of a window for access in memory. Data can be written to the GRAM. The written data is from the address specified by VSA8-0 to the address specified by VEA8-0. Note that an address must be set before RAM data are written. Ensure 000h ≤ VSA8-0 ≤ VEA8-0 ≤ 13Fh.

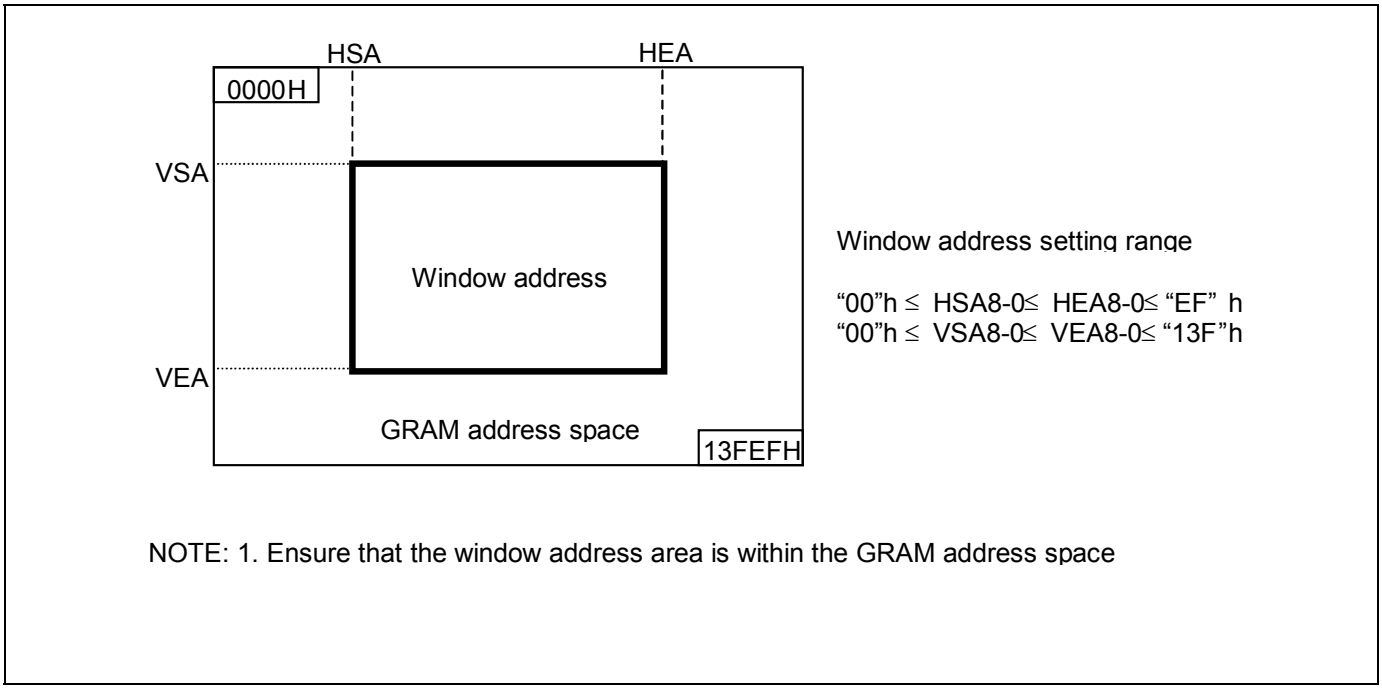


Figure 7.2.7 Window Address Setting Range

MDDI Wake Up Control (R50H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	WAKE_EN
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

WAKE_EN: When WAKE_EN is 1, client initiated wake-up is enabled. But parameter data IB[15:1] must be “0000h”, otherwise, client initiated wake-up is disabled.

MDDI Wake Start Position (R51H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	WKL7	WKL6	WKL5	WKL4	WKL3	WKL2	WKL1	WKL0	0	0	0	0	WKF3	WKF2	WKF1	WKF0
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

WKF3-0: When client initiated wake-up is used at MDDI, the frame position that data is updated is set by the value of WKF 3-0. The range of WKF is from ‘0000’ to ‘1111’. If WKF is ‘0000’, data is updated at the first frame, and if “1111” data update starts after 16th frame.

WKL7-0: When client initiated wakeup is used at MDDI, data is updated at the line the value of WKL7-0 in the frame that is set by WKL7-0. The WKL supports from ‘00h’ to ‘FFh’. If WKL is ‘00h’, data is updated at the first line, and if WKL is ‘FFh’, data update starts at the 256th line.

Setting of WFK and WKL is needed for client-initiated link wake-up. For example, WKF is “0010” and WKL is “0001”, data is updated at second line of third frame.

Sub Panel Control 1 (R52H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	MODE_SEL [1:0]		SUB_IM[1:0]	
default	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

MODE_SEL1-0 : set the STN and MPU interfaces

MODE_SEL1	MODE_SEL0	Interface
0	0	STN mode
0	1	Setting prohibit
1	0	TFT 80 mode
1	1	TFT 68 mode

SUB_IM1-0: set the bus width of sub-panel interface.

SUB_IM1	SUB_IM0	Interface
0	0	18bit
0	1	9bit
1	0	16bit
1	1	8bit

Sub Panel Control 2 / 3 (R53H / R54H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	SUB_SEL[7:0]							
default	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0
W	1	0	0	0	0	0	0	0	0	SUB_WR[7:0]							
default	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0

SUB_SEL: SUB_SEL is the index of main/sub panel selection. Initial value of SUB_SEL is ‘7Ah’. In MDDI mode, If written register address is ‘7Ah’ (initial state: SUB_SEL is ‘7Ah’) and register data is ‘0001h’, then main panel is selected, and if that is “0000h”, then sub panel is selected. Using SUB_SEL register, Main / Sub panel selection index change is possible.

SUB_WR: SUB_WR is the index of sub panel data write. Initial value of SUB_WR is ‘22h’. When MDDI host transfer GRAM data to sub panel driver IC via video stream packet, SUB_WR (initially 22h), index for GRAM access is automatically transferred before GRAM data transfer. When sub panel driver IC uses other address, 22h address have to be changed. Then user can change SUB_WR value from 22h to other value

GPIO Control (R55H / R56H / R57H / R58H / R59H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	GPIO_DATA[9:0]									
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W	1	0	0	0	0	0	0	GPIO_CON[9:0]									
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W	1	0	0	0	0	0	0	GPIO_CLR[9:0]									
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W	1	0	0	0	0	0	0	GPIO_EN[9:0]									
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W	1	0	0	0	0	0	0	GPIO_POL[9:0]									
default	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

GPIO_DATA: GPIO input data value. When GPIO is input mode, GPIO value is set to the register.

GPIO_CON: Control of GPIO PAD direction, When GPIO_CON is “0”, then GPIO is input mode, and when GPIO_CON is “1”, then GPIO is output mode.

GPIO_CLR: After GPIO has an interrupt, GPIO_CLR clears specified GPIO interrupt.

GPIO_EN: Enable specified GPIO interrupt. When GPIO is set input, if GPIO_EN is “1”, it acts as enable internal interrupt.

GPIO_POL: Control polarity setting of GPIO interrupt. If the bit is set to “1”, GPIO interrupt happens at rising edge of GPIN, If set to “0”, it happens at falling edge.

For more information about these registers, refer to GPIO CONTROL section

MTP Control (R60H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	0	0	0	0	0	0	0	0	0	0	0	0	MTP_ LOAD	MTP_ WRB	MTP_ SEL	MTP_ ERB
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

MTP_LOAD: If MTP_LOAD is set high (more 80ns), then MTP data latch from MTP cells to MTP port. Default is Low.

MTP_WRB: MTP Program Enable signal, Low active, it is only usable in STB or SLP mode. Default is high. R62h (Test Key command) should be set '8C'h before this command.

MTP_SEL: MTP value (MTP VCOMH) or Instruction value (R15H VCOMH) selection, If MTP_SEL = 1, VCOMH of MTP Data is selected, else MTP_SEL = 0, the value of Instruction Register VCOMH (R15h) is selected.

MTP_ERB: MTP initial (Erase) mode set. If MTP_ERB = 0, MTP data are initialized to all zero. R62h (Test Key command) should be set '8C'h before this command.

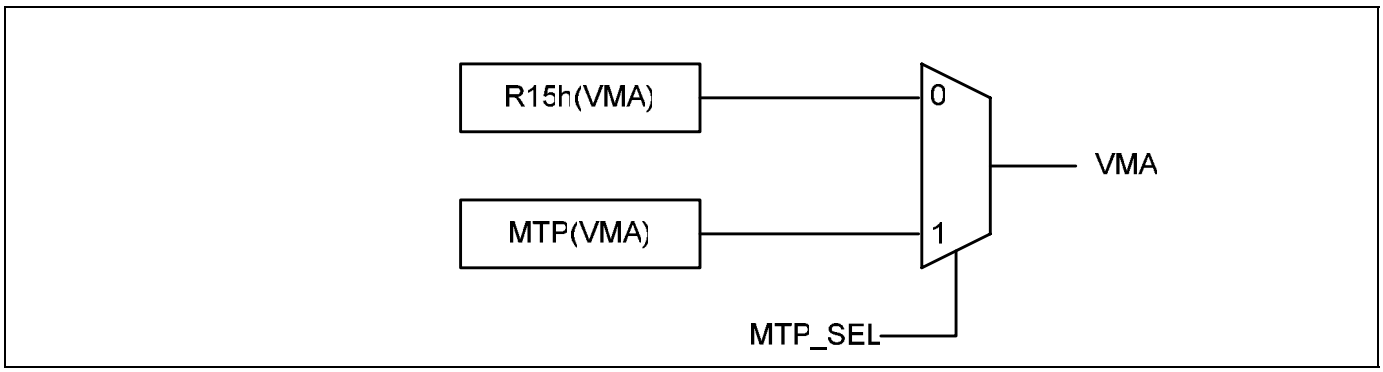


Figure 7.2.8 Relation between R15h and MTP

NOTES: In MDDI Mode, it doesn't work at STB Mode. So, it is only active at SLP Mode in MDDI

MTP VCOMH READ (R61H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB1
W	0	0	0	0	0	0	0	0	0	0	MTP _D6	MTP_ D5	MTP_ D4	MTP_ D3	MTP_ D2	MTP _D1	MTP_ D1
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This command reads the VCOM MTP Read bits.

Read 7bit data from MTP cells. D6 is protection bit which should be high, when MTP is programming. If MSB set to high, it cannot be write-protective. If you want to re-write, first Initialize MTP, then MTP D6 set to low.

MTP Bit	Descriptions
MTP_D6	Protection
MTP_D5	VMA[5]
MTP_D4	VMA[4]
MTP_D3	VMA[3]
MTP_D2	VMA[2]
MTP_D1	VMA[1]
MTP_D0	VMA[0]

MTP Test Key Command (R62H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This command is a key of some operations (ex. MTP_ERB, MTP_WRB). If it is not matched with ‘8C’, then some MTP command doesn’t operate.

GOE Start / End Timing Control (R70H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	0	0	0	0	0	0	GOST[1:0]		0	0	0	GOED[4:0]				
default	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	1	1

GOST: Control of register bits for gate enable start timing. Set up in the range 01H ≤ GOST [1:0] ≤ 03H

GOST [1:0]		OSC clock (1 Mhz)	DOTCLK (18/16-Bit, 5Mhz)
0	0	0 clock cycle	0 clock cycle
0	1	1 clock cycle	1 clock cycle x 4
1	0	2 clock cycle	2 clock cycle x 4
1	1	3 clock cycle	3 clock cycle x 4

GOED: Control of register bits for gate enable end timing. Set up in the range GOST< GOED ≤ RTN

GOED [4:0]					OSC clock (1 Mhz)	DOTCLK (18/16-Bit, 5Mhz)
0	0	0	0	0	32 clock cycle	32 clock cycle x 4
0	0	0	0	1	33 clock cycle	33 clock cycle x 4
0	0	0	1	0	34 clock cycle	34 clock cycle x 4
0	0	0	1	1	35 clock cycle	35 clock cycle x 4
0	0	1	0	0	36 clock cycle	36 clock cycle x 4
0	0	1	0	1	37 clock cycle	37 clock cycle x 4
0	0	1	1	0	38 clock cycle	38 clock cycle x 4
0	0	1	1	1	39 clock cycle	39 clock cycle x 4
0	1	0	0	0	40 clock cycle	40 clock cycle x 4
0	1	0	0	1	41 clock cycle	41 clock cycle x 4
0	1	0	1	0	42 clock cycle	42 clock cycle x 4
0	1	0	1	1	43 clock cycle	43 clock cycle x 4
0	1	1	0	0	44 clock cycle	44 clock cycle x 4
0	1	1	0	1	45 clock cycle	45 clock cycle x 4
0	1	1	1	0	46 clock cycle	46 clock cycle x 4
0	1	1	1	1	47 clock cycle	47 clock cycle x 4
1	0	0	0	0	48 clock cycle	48 clock cycle x 4
1	0	0	0	1	49 clock cycle	49 clock cycle x 4
1	0	0	1	0	50 clock cycle	50 clock cycle x 4
1	0	0	1	1	51 clock cycle	51 clock cycle x 4
1	0	1	0	0	52 clock cycle	52 clock cycle x 4
1	0	1	0	1	53 clock cycle	53 clock cycle x 4
1	0	1	1	0	54 clock cycle	54 clock cycle x 4
1	0	1	1	1	55 clock cycle	55 clock cycle x 4
1	1	0	0	0	56 clock cycle	56 clock cycle x 4
1	1	0	0	1	57 clock cycle	57 clock cycle x 4
1	1	0	1	0	58 clock cycle	58 clock cycle x 4
1	1	0	1	1	59 clock cycle	59 clock cycle x 4
1	1	1	0	0	60 clock cycle	60 clock cycle x 4
1	1	1	0	1	61 clock cycle	61 clock cycle x 4
1	1	1	1	0	62 clock cycle	62 clock cycle x 4
1	1	1	1	1	63 clock cycle	63 clock cycle x 4

NOTE: Don't set over the range of setting RTN. Also, make sure that GOST + GOED < 64 clocks.

GSP Clock Delay Control (R71H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	GSP_DLY[3:0]			
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GSP_DLY: Control the starting of gate start pulse.

GSP_DLY[3:0]				OSC clock (1 Mhz)	DOTCLK (18/16-Bit, 5Mhz)
0	0	0	0	0 clock cycle	0 clock cycle
0	0	0	1	1 clock cycle	1 clock cycle x 4
0	0	1	0	2 clock cycle	2 clock cycle x 4
0	0	1	1	3 clock cycle	3 clock cycle x 4
0	1	0	0	4 clock cycle	4 clock cycle x 4
0	1	0	1	5 clock cycle	5 clock cycle x 4
0	1	1	0	6 clock cycle	6 clock cycle x 4
0	1	1	1	7 clock cycle	7 clock cycle x 4
1	0	0	0	8 clock cycle	8 clock cycle x 4
1	0	0	1	9 clock cycle	9 clock cycle x 4
1	0	1	0	10 clock cycle	10 clock cycle x 4
1	0	1	1	11 clock cycle	11 clock cycle x 4
1	1	0	0	12 clock cycle	12 clock cycle x 4
1	1	0	1	13 clock cycle	13 clock cycle x 4
1	1	1	0	14 clock cycle	14 clock cycle x 4
1	1	1	1	15 clock cycle	15 clock cycle x 4

R Source Output Start Point (R72H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	R_STP[2:0]		
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

R_STP: The Start timing of the RED signal output from SOURCE in setup.

R_STP[2:0]			OSC clock (1 Mhz)	DOTCLK (18/16-Bit, 5Mhz)
0	0	0	1 clock cycle	1 clock cycle x 4
0	0	1	5 clock cycle	5 clock cycle x 4
0	1	0	6 clock cycle	6 clock cycle x 4
0	1	1	7 clock cycle	7 clock cycle x 4
1	0	0	8 clock cycle	8 clock cycle x 4
1	0	1	9 clock cycle	9 clock cycle x 4
1	1	0	10 clock cycle	10 clock cycle x 4
1	1	1	11 clock cycle	11 clock cycle x 4

G Source Output Start Point (R73H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	G_STP[2:0]		
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

G_STP: The Start timing of the GREEN signal output from SOURCE in setup. Set up in the range R_STP < G_STP ≤ R_STP + 15 clock cycle

G_STP[2:0]			OSC clock (1 Mhz)	DOTCLK (18/16-Bit, 5Mhz)
0	0	0	8 clock cycle	8 clock cycle x 4
0	0	1	9 clock cycle	9 clock cycle x 4
0	1	0	10 clock cycle	10 clock cycle x 4
0	1	1	11 clock cycle	11 clock cycle x 4
1	0	0	12 clock cycle	12 clock cycle x 4
1	0	1	13 clock cycle	13 clock cycle x 4
1	1	0	14 clock cycle	14 clock cycle x 4
1	1	1	15 clock cycle	15 clock cycle x 4

B Source Output Start Point (R74H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	B_STP[2:0]		
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

B_STP: Control the Start timing of the GREEN signal output from SOURCE in setup. Set up in the range G_STP (R_STP + G_STP) < B_STP ≤ 15 + G_STP (R_STP + B_STP).

B_STP[2:0]			OSC clock (1 Mhz)	DOTCLK (18/16-Bit, 5Mhz)
0	0	0	8 clock cycle	8 clock cycle x 4
0	0	1	9 clock cycle	9 clock cycle x 4
0	1	0	10 clock cycle	10 clock cycle x 4
0	1	1	11 clock cycle	11 clock cycle x 4
1	0	0	12 clock cycle	12 clock cycle x 4
1	0	1	13 clock cycle	13 clock cycle x 4
1	1	0	14 clock cycle	14 clock cycle x 4
1	1	1	15 clock cycle	15 clock cycle x 4

R Mux Start Pulse and Width Timing Control (R75H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	M_RSTP[1:0]		0	0	0	0	0	M_RPW[2:0]		
default	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0

M_RSTP: Control the start timing of the catching the Red signal output. Set up in the range R_STP < M_RSTP ≤ 3 + R_STP.

M_RSTP[1:0]		OSC clock (1 Mhz)	DOTCLK (18/16-Bit, 5Mhz)
0	0	Disable	Disable
0	1	1 clock cycle	1 clock cycle x 4
1	0	2 clock cycle	2 clock cycle x 4
1	1	3 clock cycle	3 clock cycle x 4

M_RPW: Control the pulse width timing of caching the Red signal output.

M_RPW[2:0]			OSC clock (1 Mhz)	DOTCLK (18/16-Bit, 5Mhz)
0	0	0	8 clock cycle	8 clock cycle x 4
0	0	1	9 clock cycle	9 clock cycle x 4
0	1	0	10 clock cycle	10 clock cycle x 4
0	1	1	11 clock cycle	11 clock cycle x 4
1	0	0	12 clock cycle	12 clock cycle x 4
1	0	1	13 clock cycle	13 clock cycle x 4
1	1	0	14 clock cycle	14 clock cycle x 4
1	1	1	Disable	Disable

G Mux Start Pulse and Width Timing Control (R76H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	M_GSTP[1:0]		0	0	0	0	0	M_GPW[2:0]		
default	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0

M_GSTP: Control the start timing of catching the Green signal output. Set up in the range G_STP ≤ M_GSTP ≤ 3 + G_STP.

M_GSTP[1:0]		OSC clock (1 Mhz)	DOTCLK (18/16-Bit, 5Mhz)
0	0	Disable	Disable
0	1	1 clock cycle	1 clock cycle x 4
1	0	2 clock cycle	2 clock cycle x 4
1	1	3 clock cycle	3 clock cycle x 4

M_GPW: Control the pulse width of catching the Green signal output.

M_GPW[2:0]			OSC clock (1 Mhz)	DOTCLK (18/16-Bit, 5Mhz)
0	0	0	8 clock cycle	8 clock cycle x 4
0	0	1	9 clock cycle	9 clock cycle x 4
0	1	0	10 clock cycle	10 clock cycle x 4
0	1	1	11 clock cycle	11 clock cycle x 4
1	0	0	12 clock cycle	12 clock cycle x 4
1	0	1	13 clock cycle	13 clock cycle x 4
1	1	0	14 clock cycle	14 clock cycle x 4
1	1	1	Disable	Disable

B Mux Start Pulse and Width Timing Control (R77H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	M_BSTP[1:0]		0	0	0	0	0	M_BPW[2:0]		
default	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0

M_BSTP: Control the start timing of catching the Red signal output. Set up in the range B_STP < M_BSTP ≤ 3 + B_STP.

M_BSTP[1:0]		OSC clock (1 Mhz)	DOTCLK (18/16-Bit, 5Mhz)
0	0	Disable	Disable
0	1	1 clock cycle	1 clock cycle x 4
1	0	2 clock cycle	2 clock cycle x 4
1	1	3 clock cycle	3 clock cycle x 4

M_BPW: Control the pulse width of catching the Red signal output.

M_BPW[2:0]			OSC clock (1 Mhz)	DOTCLK (18/16-Bit, 5Mhz)
0	0	0	8 clock cycle	8 clock cycle x 4
0	0	1	9 clock cycle	9 clock cycle x 4
0	1	0	10 clock cycle	10 clock cycle x 4
0	1	1	11 clock cycle	11 clock cycle x 4
1	0	0	12 clock cycle	12 clock cycle x 4
1	0	1	13 clock cycle	13 clock cycle x 4
1	1	0	14 clock cycle	14 clock cycle x 4
1	1	1	Disable	Disable

Vcom Output Control (R78H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VMCHG[1:0]	
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VMCHG: Control the start timing of the Vcom signal output. Set up in the range 1 ≤ VMCHG ≤ 4.

VMCHG[1:0]		OSC clock (1 Mhz)	DOTCLK (18/16-Bit, 5Mhz)
0	0	1 clock cycle	1 clock cycle x 4
0	1	2 clock cycle	2 clock cycle x 4
1	0	3 clock cycle	3 clock cycle x 4
1	1	4 clock cycle	4 clock cycle x 4

Panel Signal Control 1 (R79H):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	LGSP_OFF	LGCLK4_OFF	LGCLK3_OFF	LGCLK2_OFF	LGCLK1_OFF	0	RGSP_OFF	RGCLK4_OFF	RGCLK3_OFF	RGCLK2_OFF	RGCLK1_OFF	R_OFF	G_OFF	B_OFF
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LGSP_OFF: GSP output is controlled. “0”: Normal operation (default), “1”: OFF

LGCLK4_OFF: GCLK4 output is controlled. “0”: Normal operation (default), “1”: OFF

LGCLK3_OFF: GCLK3 output is controlled. “0”: Normal operation (default), “1”: OFF

LGCLK2_OFF: GCLK2 output is controlled. “0”: Normal operation (default), “1”: OFF

LGCLK1_OFF: GCLK1 output is controlled. “0”: Normal operation (default), “1”: OFF

RGSP_OFF: GSP output is controlled. “0”: Normal operation (default), “1”: OFF

RGCLK4_OFF: GCLK4 output is controlled. “0”: Normal operation (default), “1”: OFF

RGCLK3_OFF: GCLK3 output is controlled. “0”: Normal operation (default), “1”: OFF

RGCLK2_OFF: GCLK2 output is controlled. “0”: Normal operation (default), “1”: OFF

RGCLK1_OFF: GCLK1 output is controlled. “0”: Normal operation (default), “1”: OFF

R_OFF: RSW output is controlled. “0”: Normal operation (default), “1”: OFF

G_OFF: GSW output is controlled. “0”: Normal operation (default), “1”: OFF

B_OFF: BSW output is controlled. “0”: Normal operation (default), “1”: OFF

Panel Signal Control 2 (R7AH):

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	LGSP_POL	LGCLK4_POL	LGCLK3_POL	LGCLK2_POL	LGCLK1_POL	0	RGSP_POL	RGCLK4_POL	RGCLK3_POL	RGCLK2_POL	RGCLK1_POL	R_POL	G_POL	B_POL
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LGSP_POL: GSP polarity is controlled. “0”: Low active pulse generation, “1”: High active pulse generation (default)

LGCLK4_POL: GCLK4 polarity is controlled. “0”: Low active pulse generation (default), “1”: High active pulse generation

LGCLK3_POL: GCLK3 polarity is controlled. “0”: Low active pulse generation (default), “1”: High active pulse generation

LGCLK2_POL: GCLK2 polarity is controlled. “0”: Low active pulse generation (default), “1”: High active pulse generation

LGCLK1_POL: GCLK1 polarity is controlled. “0”: Low active pulse generation (default), “1”: High active pulse generation

RGSP_POL: GSP polarity is controlled. “0”: Low active pulse generation, “1”: High active pulse generation (default)

RGCLK4_POL: GCLK4 polarity is controlled. “0: Low active pulse generation (default), “1”: High active pulse generation

RGCLK3_POL: GCLK3 polarity is controlled. “0: Low active pulse generation (default), “1”: High active pulse generation

RGCLK2_POL: GCLK2 polarity is controlled. “0: Low active pulse generation (default) ,“1: High active pulse generation

RGCLK1_POL: GCLK1 polarity is controlled. “0: Low active pulse generation (default), “1: High active pulse generation

R_POL: RSW polarity is controlled. “0: Low active pulse generation (default), “1”: High active pulse generation

G_POL: GSW polarity is controlled. “0: Low active pulse generation (default), “1”: High active pulse generation

B_POL: BSW polarity is controlled. “0: Low active pulse generation (default), “1”: High active pulse generation

GATE1 and GATE2 Switching Control (R97H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	CHNG	0	0	0	0	0	0	0
default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CHNG: This register swap GCLK1 signal & GCLK2 signal.

0 : normal operation

1: Swap operation

8. DC / AC CHARACTERISTICS

8.1 ABSOLUTE MAXIMUM RATINGS

Table 8.1.1 Absolute Maximum Rating

(VSS = 0 V)

Item	Symbol	Rating	Unit
Supply voltage	VDD – VSS	-0.3 ~ 3.0	V
Supply voltage 3	VDD3 – VSS	-0.3 ~ 5.0	V
Supply voltage for step-up circuit	VCI – VSS	-0.3 ~ 5.0	V
LCD Supply Voltage range	AVDD – VSS	-0.3 ~ 6.5	V
	|VGH – VGL|	-0.3 ~ 35	V
Input Voltage range	Vin	-0.3 to VDD3 +0.5	V
Operating temperature	T_{opr}	-40 ~ 85	°C
Storage temperature	T_{stg}	-55 ~ 110	°C

NOTES:

1. Absolute maximum rating is the limit value beyond which the IC may be broken. They do not assure operations.
2. Operating temperature is the range of device-operating temperature. They do not guarantee chip performance.
3. Absolute maximum rating is guaranteed when our company's package used.

8.2 LCD DRIVER DC CHARACTERISICS

Table 8.2.1 DC Characteristics

(VSS = 0 V)

Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
Operating voltage	VDD		1.4	1.5	1.6	V	*1
	VDD3		1.65	-	3.3	V	*1
LCD driving voltage	VGH		7.5	-	16.0	V	
	VGL		-11	-	-5.5	V	
	VGLROUT		-10.5	-	-5.0	V	
	AVDD		3.4	-	6.0	V	
	GVDD		3.	-	5.0	V	
Input high voltage	VIH		0.8*VDD3	-	VDD3	V	*2
Input low voltage	VIL		0	-	0.2*VDD3	V	*2
Output high voltage	VOH	IOH = -0.5mA	0.7*VDD3	-	VDD3	V	*3
Output low voltage	VOL	IOL = 0.5mA	0	-	0.3*VDD3	V	*3
Input leakage current	IIL	VIN = VSS or VDD3	-1.0		1	uA	*2
Output leakage current	IOL	VIN = VSS or VDD3	-3.0		3.0	uA	*3
Operating frequency	fosc	Frame freq. = 70 Hz Display line = 320		1.0		MHz	*4
External supply voltage	VCI		2.5		3.3	V	
1st step-up input voltage	VCI1		1.75		3.0	V	
1st step-up output efficiency	AVDD	ILOAD = 4 mA	90	95	100	%	
2nd step-up output efficiency	VGH	ILOAD = 0.1 mA	90	95	100	%	
3rd step-up output efficiency	VGL	ILOAD = 0.1 mA	90	95	100	%	

NOTES:

1. VSS = 0V.
2. Applied pins; IM3-0, CSB, E_RDB, RW_WRB, RS, DB0 to DB17, PD0 to PD17, PREGB, RESETB.
3. Applied pins; DB0 to DB17
4. Target frame frequency = 70 Hz, Display line = 320, Back porch = 4, Front porch = 4 Internal RTN [4:0] register = “0_1011” (You Can measure OSC (fosc) or CL1 (fosc/43))

Table 8.2.2 DC Characteristics for LCD Driver Outputs

(VDD = 1.5 V, VDD3 = 3.0V, VSS = 0V)

Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
LCD gate driver output On resistance	Ron	VGH=16.0V, VGL=-11.0V VGLROUT = -10.5V			2.5	kohm	
LCD mux driver output On resistance	Ron				1.5	kohm	
LCD source driver delay	tSD	SAP = "001"	-	-	8.5	us	*1
		SAP = "010"	-	-	7.5	us	*1
		SAP = "011"	-	-	6.5	us	*1
		SAP = "100"	-	-	6	us	*1
		SAP = "101"			5.5	us	*1
		SAP = "110"			5	us	*1
		SAP = "111"			4.0	us	*1
Output voltage deviation (Mean value)	ΔV_O	$4.2V \leq V_{SO}$	-	±20	±55	mV	*2
		$0.8V < V_{SO} < 4.2V$	-	±10	±25	mV	*2
		$V_{SO} \leq 0.8V$	-	±20	±55	mV	*2
LCD source driver output voltage range	V_{SO}	Ta = 25 °C	GVDD-0.1	-	GVDD+0.1	V	-
LCD source driver output On resistance	Ronp	AVDD=5.0V GVDD=4.5V	-	-	20	kΩ	-
LCD source driver output On resistance	Ronn	AVDD=5.0V VGS=GNDV	-	-	20	kΩ	-
Current consumption during standby mode	Ivdd3-stby	Standby mode, VCI=3.0V Ta = 25 °C	-	-	5	uA	-
	Ivci-stby		-	-	25	uA	-
Current consumption during sleep mode	Ivdd3-sleep	Sleep mode, VCI=3.0V Ta = 25 °C	-	-	200	uA	-
	Ivci-sleep		-	-	100	uA	-
Current consumption during normal operation	IVDD3	100pF load, Ta = 25 °C VC=010, DC=011, VR1C = 1100, VR2C = 1100, VGLRC =10110, VRH =111111 VCM=111111 VML=111111		-	200	uA	-
	IVCI		-	-	8.8	mA	-

NOTES:

1. AVDD = 5.5V, GVDD = 5.0V, Ta = 25℃
   tSD is measured on the time to reach Vtarget (-/+ 5mV).
   TSD: LCD Source driver delay
   tSD = 1 / [Frame Freq. x {The number of raster-row + The number of blank period (FP+BP)}] – The marginal time for pixel load charge

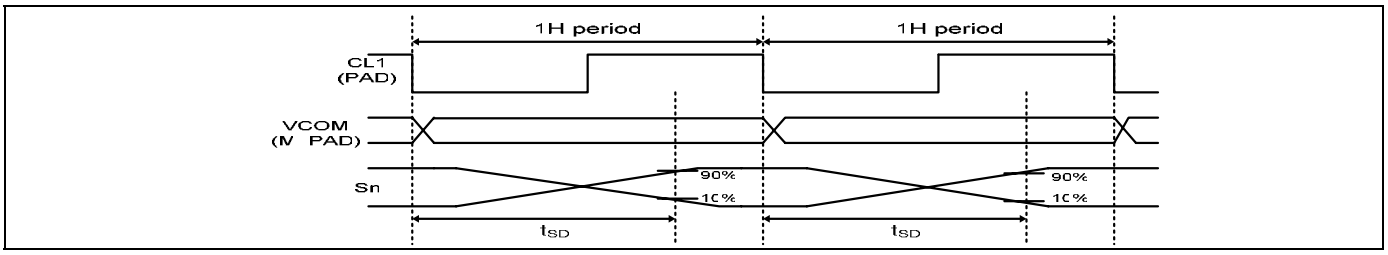


Figure 8.2.1 LCD Source Driver Delay

2. Vso the output voltage of analog output pins S1 to S240

8.3 CPU / RGB / SERIAL INTERFACE AC CHARACTERISTICS

8.3.1 68-SYSTEM 18-/16-/9-/8-BIT INTERFACE

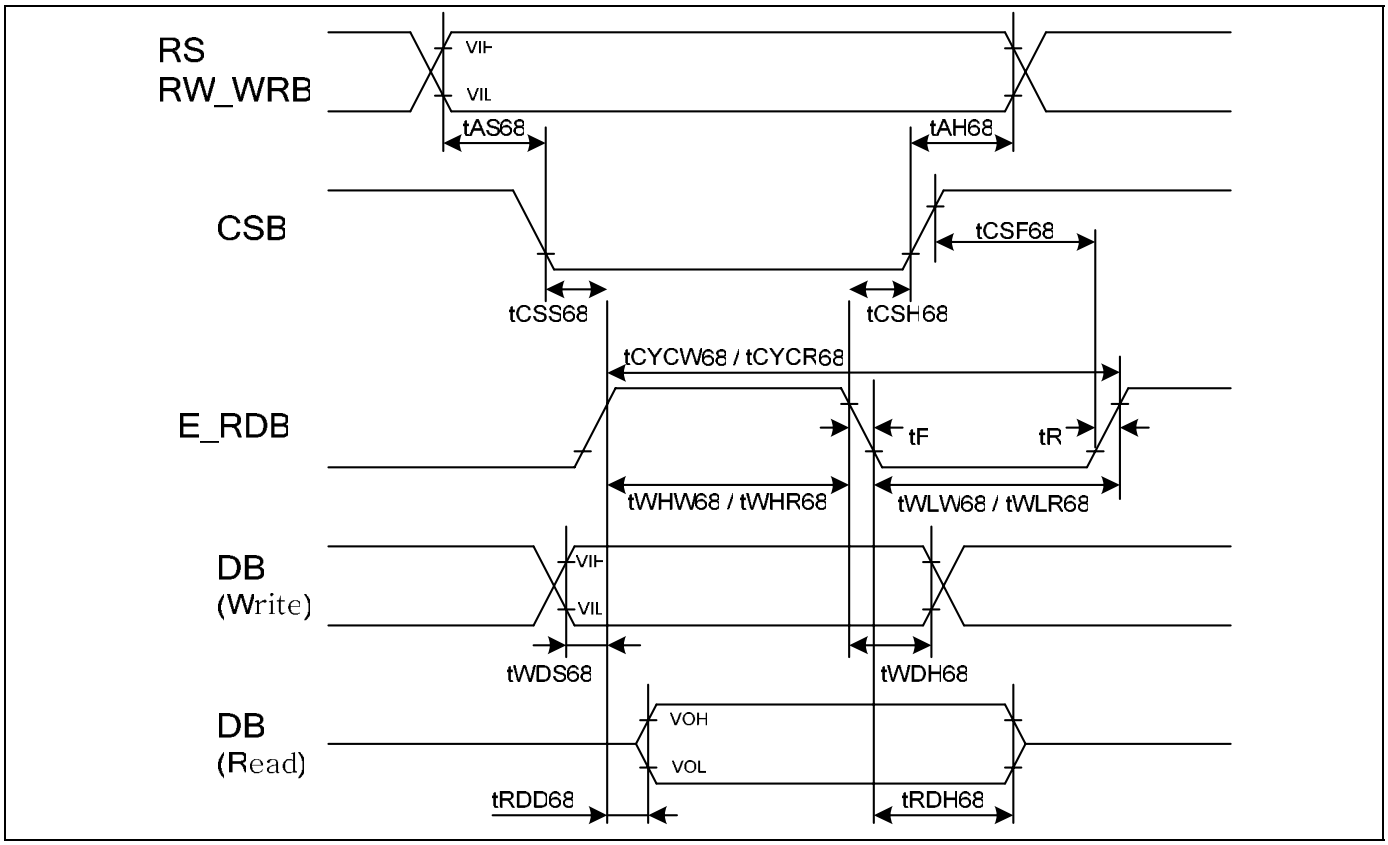


Figure 8.3.1.1 AC Timing Parameter and Timing Diagram of 68-system interface

Table 8.3.1.1 AC Timing Characteristics

(VDD = 1.5 V, VDD3 = 1.65 to 3.3V, T_A = -40 to +85 °C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Address setup time	tAS68	RS ~ CSB RW_WRB ~ CSB	5	-	ns
Address hold time	tAH68		5	-	ns
Chip select setup time	tCSS68	CSB ~ E_RDB	5	-	ns
Chip select holed time	tCSH68		5	-	ns
Chip select wait time	tCSF68		10	-	ns
Write enable period	tCYCW68	E_RDB when RW_WRB = 0	65	-	ns
Write enable high pulse width	tWHW68		22.5	-	ns
Write enable low pulse width	tWLW68		22.5	-	ns
Read enable period	tCYCR68	E_RDB when RW_WRB = 1	400	-	ns
Read enable high pulse width	tWHR68		190	-	ns
Read enable low pulse width	tWLR68		190	-	ns
Write data setup time	tWDS68	DB ~ E_RDB	10	-	ns
Write data hold time	tWDH68		10	-	ns
Read data delay time	tRDD68	DB ~ E_RDB	-	160	ns
Read data hold time	tRDH68		5	40	ns
Rising time	tR	All signals	-	10	ns
Falling time	tF		-	10	ns

8.3.2 80-SYSTEM 18-/16-/9-/8-BIT INTERFACE

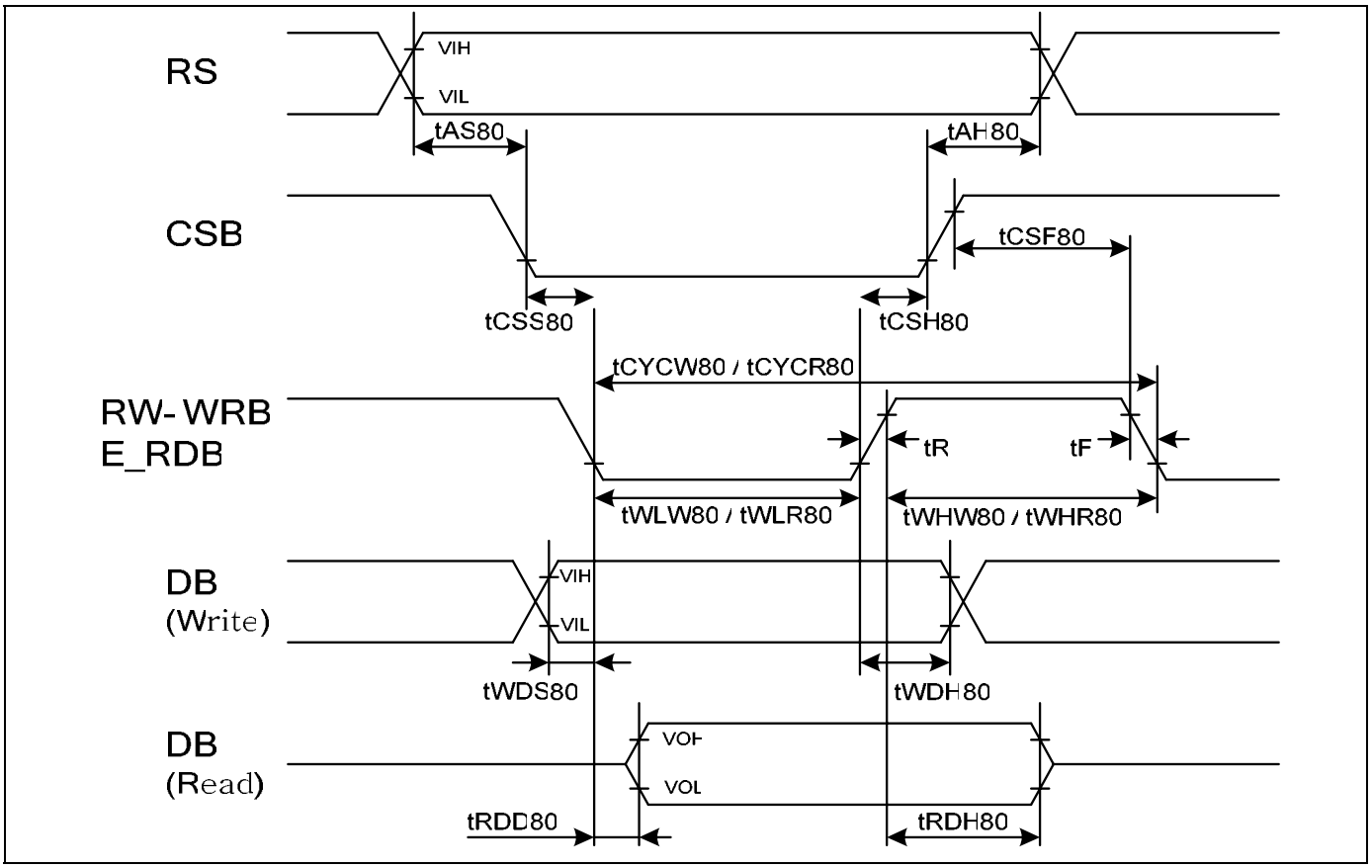


Figure 8.3.2.1 AC Timing Parameter and Timing Diagram of 80-system interface

Table 8.3.2.1 AC Timing Characteristics

(VDD = 1.5 V, VDD3 = 1.65 to 3.3V, T_A = -40 to +85 °C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Address setup time	tAS80	RS ~ CSB	5	-	ns
Address hold time	tAH80		5	-	ns
Chip select setup time	tCSS80	CSB ~ RW_WRB CSB ~ E_RDB	5	-	ns
Chip select holed time	tCSH80		5	-	ns
Chip select wait time	tCSF80		10	-	ns
Write enable period	tCYCW80	RW_WRB	65	-	ns
Write enable low pulse width	tWLW80		22.5	-	ns
Write enable high pulse width	tWHW80		22.5	-	ns
Read enable period	tCYCR80	E_RDB	400	-	ns
Read enable low pulse width	tWLR80		190	-	ns
Read enable high pulse width	tWHR80		190	-	ns
Write data setup time	tWDS80	DB ~ RW_WRB	5	-	ns
Write data hold time	tWDH80		5	-	ns
Read data delay time	tRDD80	DB ~ E_RDB	10	-	ns
Read data hold time	tRDH80		10	-	ns
Rising time	tR	All signals	-	160	ns
Falling time	tF		5	40	ns

8.4 SERIAL PERIPHERAL INTERFACE

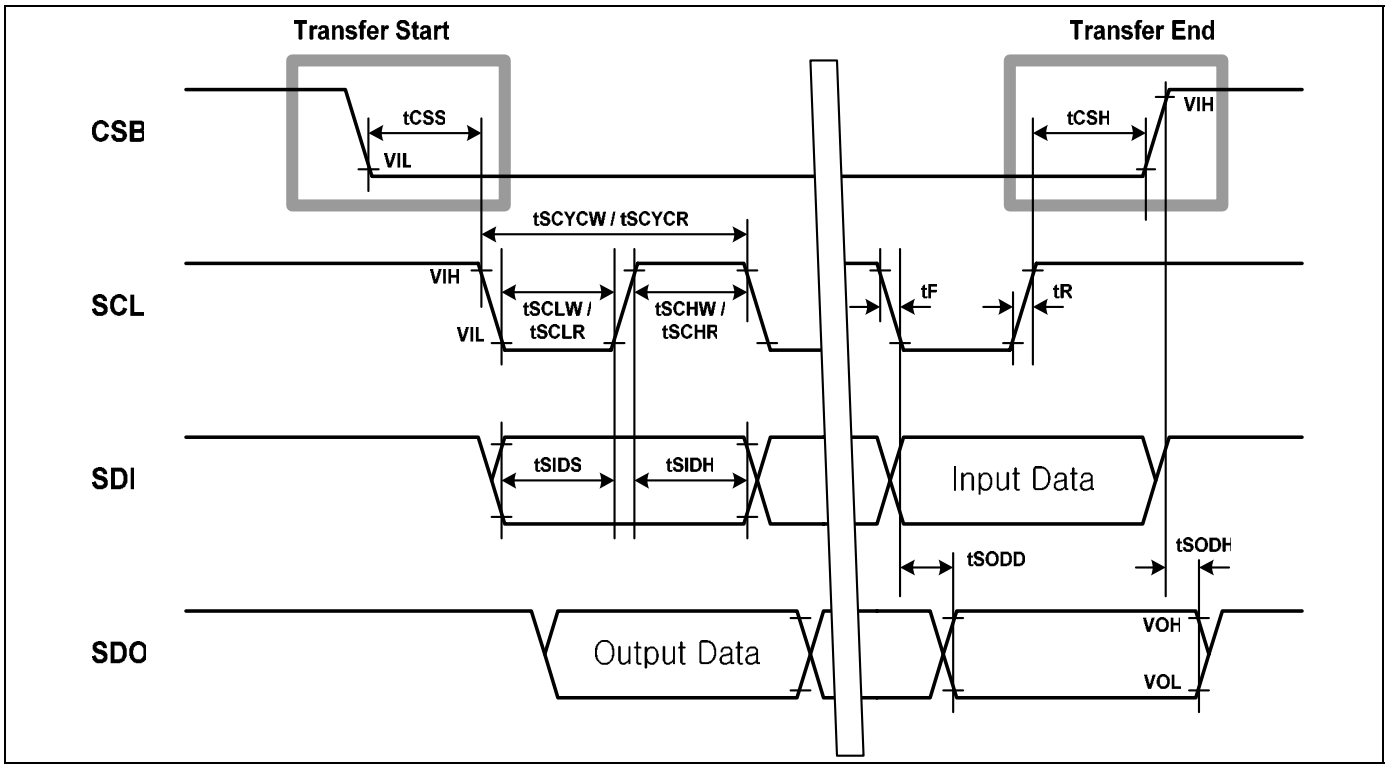


Figure 8.4.1 AC Timing Parameter and Timing Diagram of Serial Peripheral Interface

Table 8.4.1 AC Timing Characteristics

(VDD = 1.5 V, VDD3 = 1.65 to 3.3V, T_A = -40 to +85 °C)

Characteristic		Symbol	specification		Unit
			Min.	Max.	
Serial clock cycle time	Write	tSCYCW	130	-	ns
	Read	tSCYCR	250		
Serial clock rise / fall time		tR, tF	-	10	ns
Pulse width high	Write	tSCHW	55	-	ns
	Read	tSCHR	115	-	ns
Pulse width low	Write	tSCLW	55	-	ns
	Read	tSCLR	115	-	ns
Chip Select setup time		tCSS	20	-	ns
Chip Select hold time		tCSH	60	-	ns
Serial input data setup time		tSIDS	30	-	ns
Serial input data hold time		tSIDH	30	-	ns
Serial output data delay time		tSODD	-	130	ns
Serial output data hold time		tSODH	5	-	ns

8.5 RGB INTERFACE

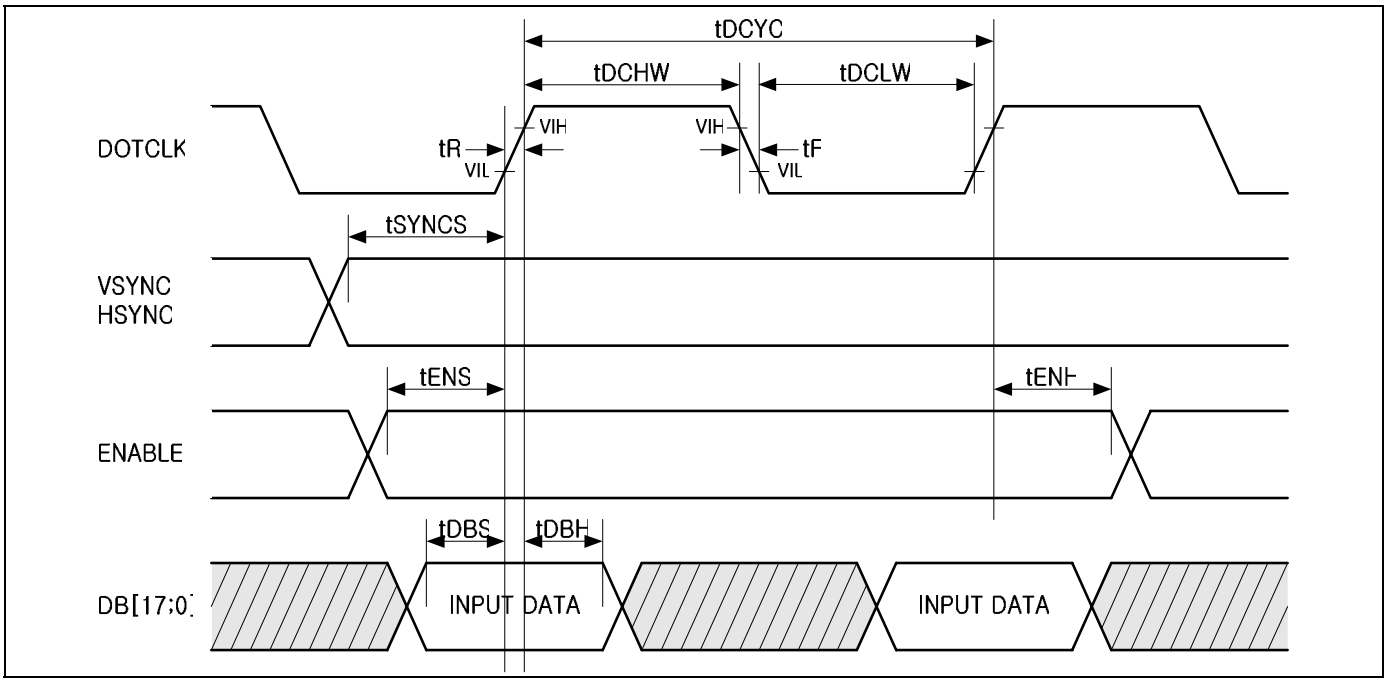


Figure 8.5.1 AC Timing Parameter and Timing Diagram of RGB Interface

Table 8.5.1 AC Timing Characteristics

(VDD = 1.5 V, VDD3 = 1.65 to 3.3V, T_A = -40 to +85 °C)

Characteristic	Symbol	Normal Mode				Unit
		18/16bit RGB interface		6bit RGB interface		
		Min.	Max.	Min.	Max.	
DOTCLK cycle time	tDCYC	100	-	55	-	ns
DOTCLK rise / fall time	tR, tF	-	10		10	ns
DOTCLK Pulse width high	tDCHW	40	-	17.5	-	ns
DOTCLK Pulse width low	tDCLW	40	-	17.5	-	ns
VSYNC/HSYNC setup time	tsyncs	15	-	15	-	ns
ENABLE setup time	tENS	15	-	15	-	ns
ENABLE hold time	tENH	7	-	7	-	ns
DB data setup time	tDBS	15	-	15	-	ns
DB data hold time	tDBH	7	-	7	-	ns

8.6 RESET TIMING

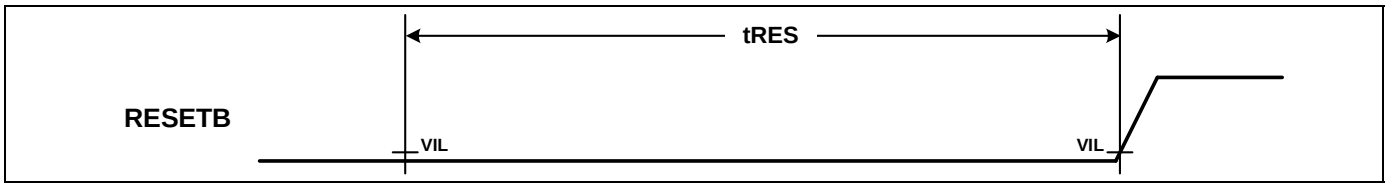


Figure 8.6.1 AC Timing Parameter and Timing Diagram of RESET

Table 8.6.1 AC Characteristics of RESET

(VDD = 1.5 V, VDD3 = 1.65 to 3.3V, T_A = -40 to +85 °C)

Characteristic	Symbol	Min.	Max.	Unit
Reset low pulse width	tRES	15	-	us

8.7 MDDI IO DC / AC CHARACTERISTICS

Table 8.7.1 Data / Strobe Rx DC Characteristics

Parameter	Description	MIN	TYP	MAX	Unit	Note
V_{IT+}	Receiver differential input high threshold voltage. Above this differential voltage the input signal shall be interpreted as a logic one level.			50	mV	
V_{IT-}	Receiver differential input low threshold voltage. Below this differential voltage the input signal shall be interpreted as a logic zero level.	-50			mV	
V_{IT+}	Receiver differential input high threshold voltage (offset for hibernation wake-up). Above this differential voltage the input signal shall be interpreted as a logic-one level.		125	175	mV	
V_{IT-}	Receiver differential input low threshold voltage (offset for hibernation wake-up). Below this differential voltage the input signal shall be interpreted as logic zero level.	75	125		mV	
$V_{Input-Range}$	Allowable receiver input voltage range with respect to client ground.	0		1.65	V	
R_{term}	Parallel termination resistance value	98	100	102	Ω	

Table 8.7.2 Data/Strobe Rx AC Characteristics

Parameter	Description	MIN	TYP	MAX	Unit	Note
V_{IT+}	Receiver differential input high threshold voltage in AC condition.			100	mV	
V_{IT-}	Receiver differential input low threshold voltage in AC condition.	-100			mV	

Table 8.7.3 Driver Electrical DC Characteristics

Parameter	Description	MIN	TYP	MAX	Unit	Note
$I_{diffabs}$	Absolute driver differential output current range (Current through the termination resistor)	2.5		4.5	mA	R_{term}= 100 Ω
$V_{out-rng-int}$	Single-ended driver output voltage range with respect to ground, internal mode	0.35		1.60	V	Under all conditions, including double-drive

NOTE: Please refer to VESA specification Ver 1.0

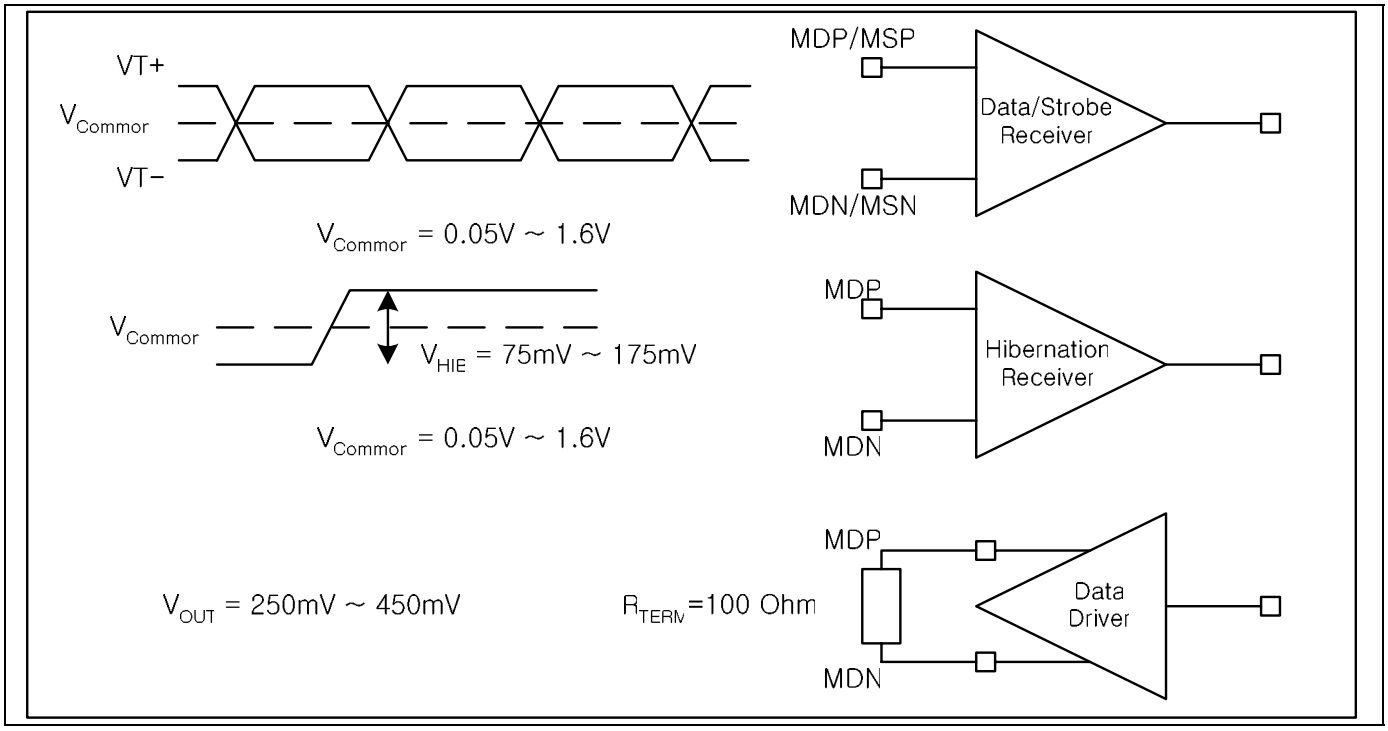


Figure 8.7.1 MDDI Receiver, Driver Electrical Diagram

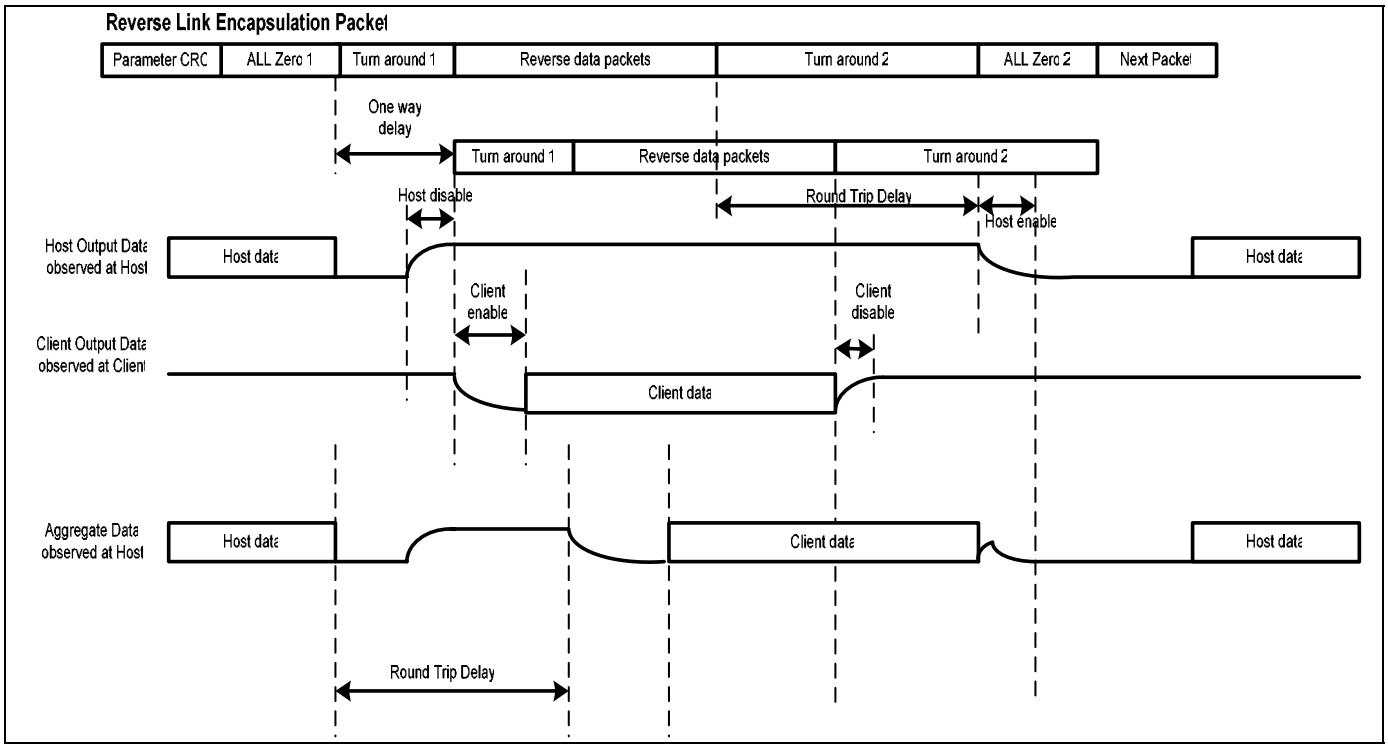


Figure 8.7.2 Host Enable / Disable Time and Client Enable / Disable Time Diagram

NOTES:

1. tBIT= 1 / Link_Data_Rate, where Link_Data_Rate is the bit rate of a single data pair
(For example, if the average forward link bit rate is 200Mbps, then tBIT= 1 / 200Mbps = 5ns)
2. These specifications are from VESA specification Ver 1.0.

8.8 SUB PANEL SIGNAL CHARACTERISTICS

Sub panel timing is described below. If 9/8 bit mode is used, each characteristics of sub panel timing is increased by 2 times, and Register writing packet and Memory writing packet have some differences.

Table 8.8.1 Sub panel signal characteristics

(k = MDDI speed (Mbps), 18bit 80 mode)

Characteristic	Symbol	Specification (Register)		Specification (Memory)		Unit
		Min.	Max.	Min.	Max.	
Cycle time	tCYCW80	10*(2000/k)	-	8*(2000/k)	-	ns
Pulse rise / fall time	**tR, tF	-	8	-	8	
Pulse width low	tWLW80	4*(2000/k) - 8	-	4*(2000/k) - 8	-	
Pulse width high	tWHW80	6*(2000/k)-8	-	4*(2000/k) - 8	-	
RW, RS and CSB setup time	tAS80	3*(2000/k)	-	3*(2000/k)	-	
RW, RS and CSB hold time	tAH80	3*(2000/k)	-	3*(2000/k)	-	
Write data setup time	tWDS80	5*(2000/k)	-	5*(2000/k)	-	
Write data hold time	tWDH80	3*(2000/k)	-	3*(2000/k)	-	

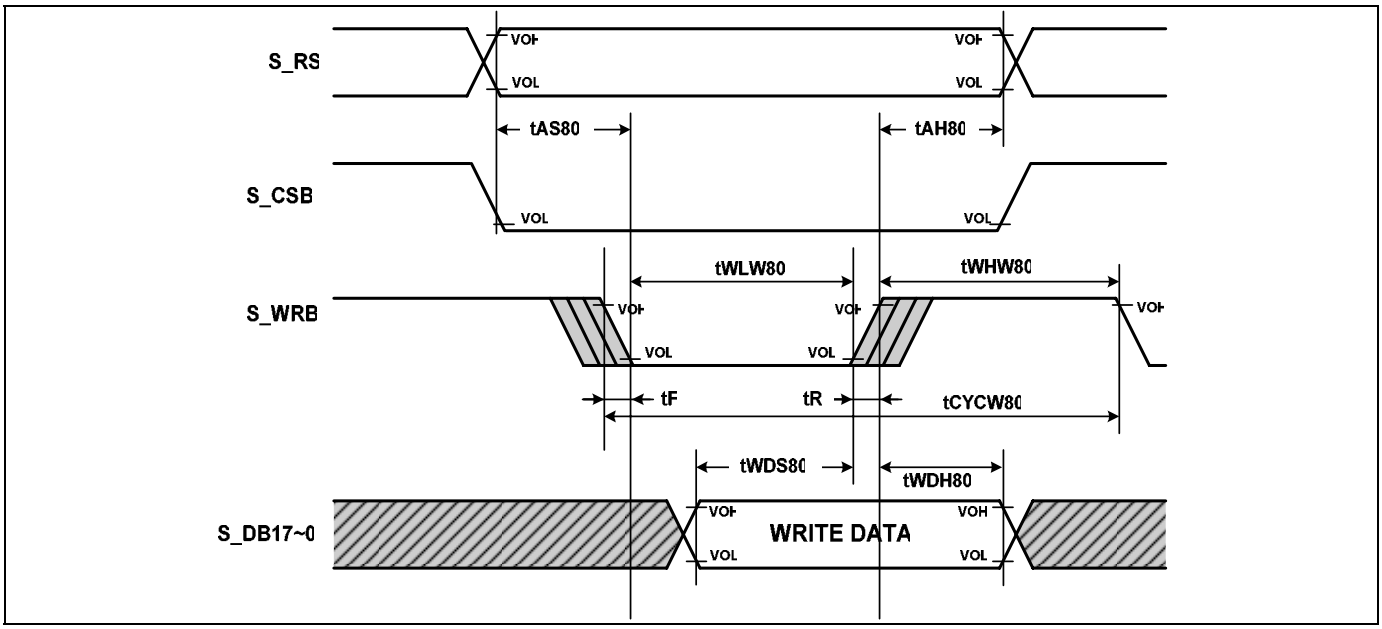


Figure 8.8.1 Sub panel signal timing(80 mode)

NOTE :

RL ≤ 200 Ω(CL ≤ 3pF)
PREGB = Low
VDD3 = 1.8 ~ 3.3V
TA = -40 ~ 85 °C

Table 8.8.2 Sub panel signal characteristics

(k = MDDI speed (Mbps), 18bit 68 mode)

Characteristic	Symbol	Specification (Register)		Specification (Memory)		Unit
		Min.	Max.	Min.	Max.	
Cycle time	tCYCW68	10*(2000/k)	-	8*(2000/k)	-	ns
Pulse rise / fall time	**tR, tF	-	8	-	8	
Pulse width low	tWLW68	6*(2000/k) - 8	-	4*(2000/k) - 8	-	
Pulse width high	tWHW68	4*(2000/k)-8	-	4*(2000/k) - 8	-	
RW, RS and CSB setup time	tAS68	3*(2000/k)	-	3*(2000/k)	-	
RW, RS and CSB hold time	tAH68	3*(2000/k)	-	3*(2000/k)	-	
Write data setup time	tWDS68	5*(2000/k)	-	5*(2000/k)	-	
Write data hold time	tWDH68	3*(2000/k)	-	3*(2000/k)	-	

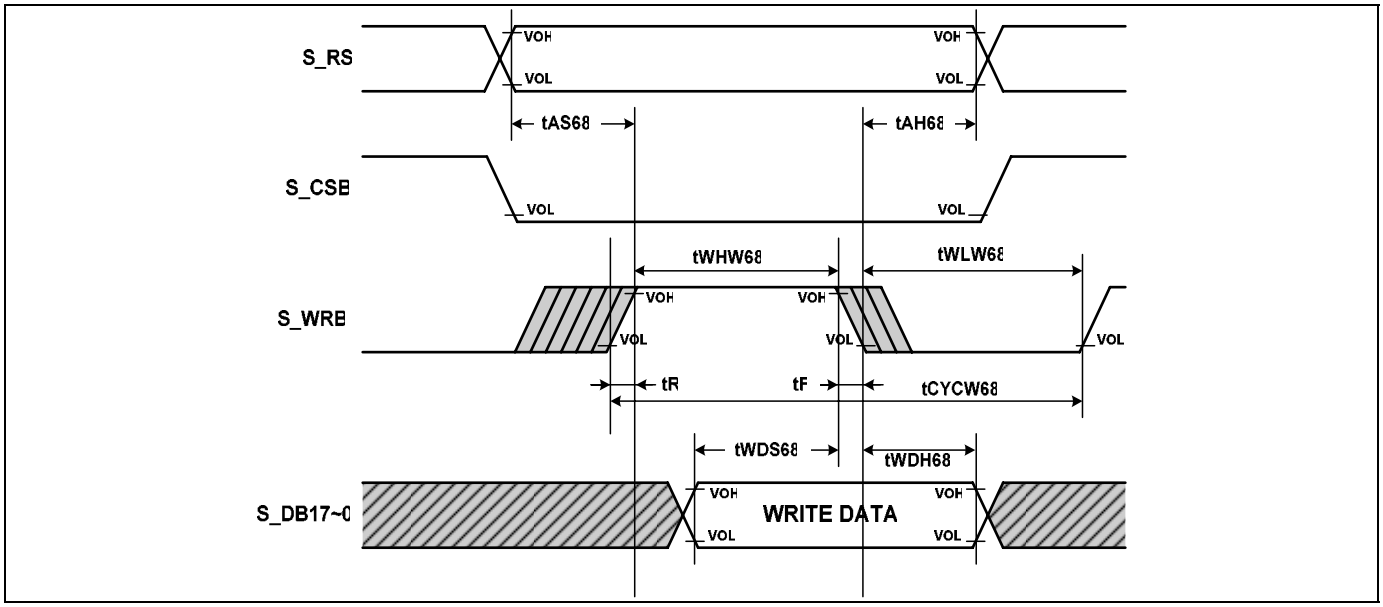


Figure 8.8.2 Sub panel signal timing(68 mode)

NOTE :

RL ≤ 200 Ω(CL ≤ 3pF)
PREGB = Low
VDD3 = 1.8 ~ 3.3V
TA = -40 ~ 85 °C

8.9 MTP DC / AC CHARACTERISTICS

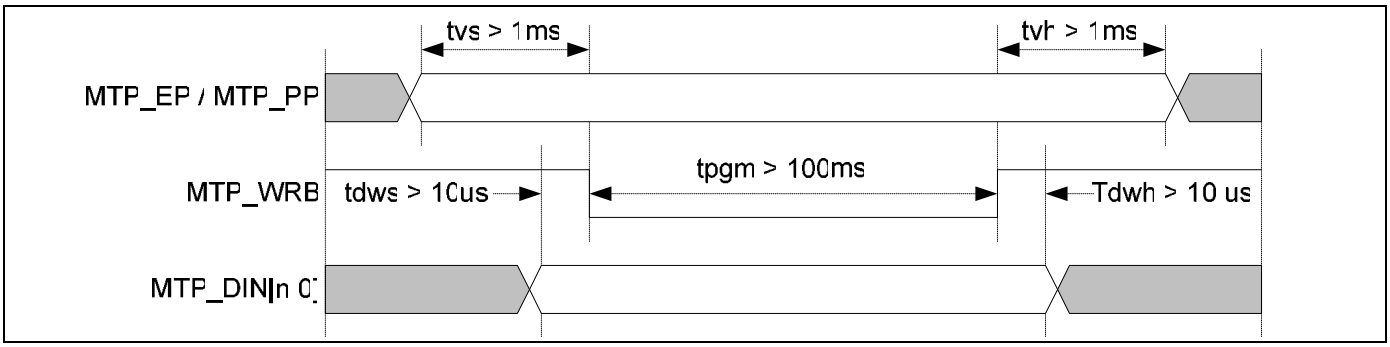


Figure 8.9.1 Voltages and Waveform for MTP Programming

Table 8.9.1 MTP Writing Time

Timing	Min	Max	Unit
tvs	1	-	ms
tvh	1	-	ms
tdws	10	-	us
tdwh	10	-	us
tpgm	100	200	ms

Table 8.9.2 MTP_EP / MTP_PP Voltage Tolerance

Item	Pgm	Min	Typ	Max	Unit
Tolerance of MTP_EP	Erase	21.0	21.5	22.0	V
	Write		0		
Tolerance of MTP_PP	Erase		0		V
	Write	17.0	17.5	18.0	

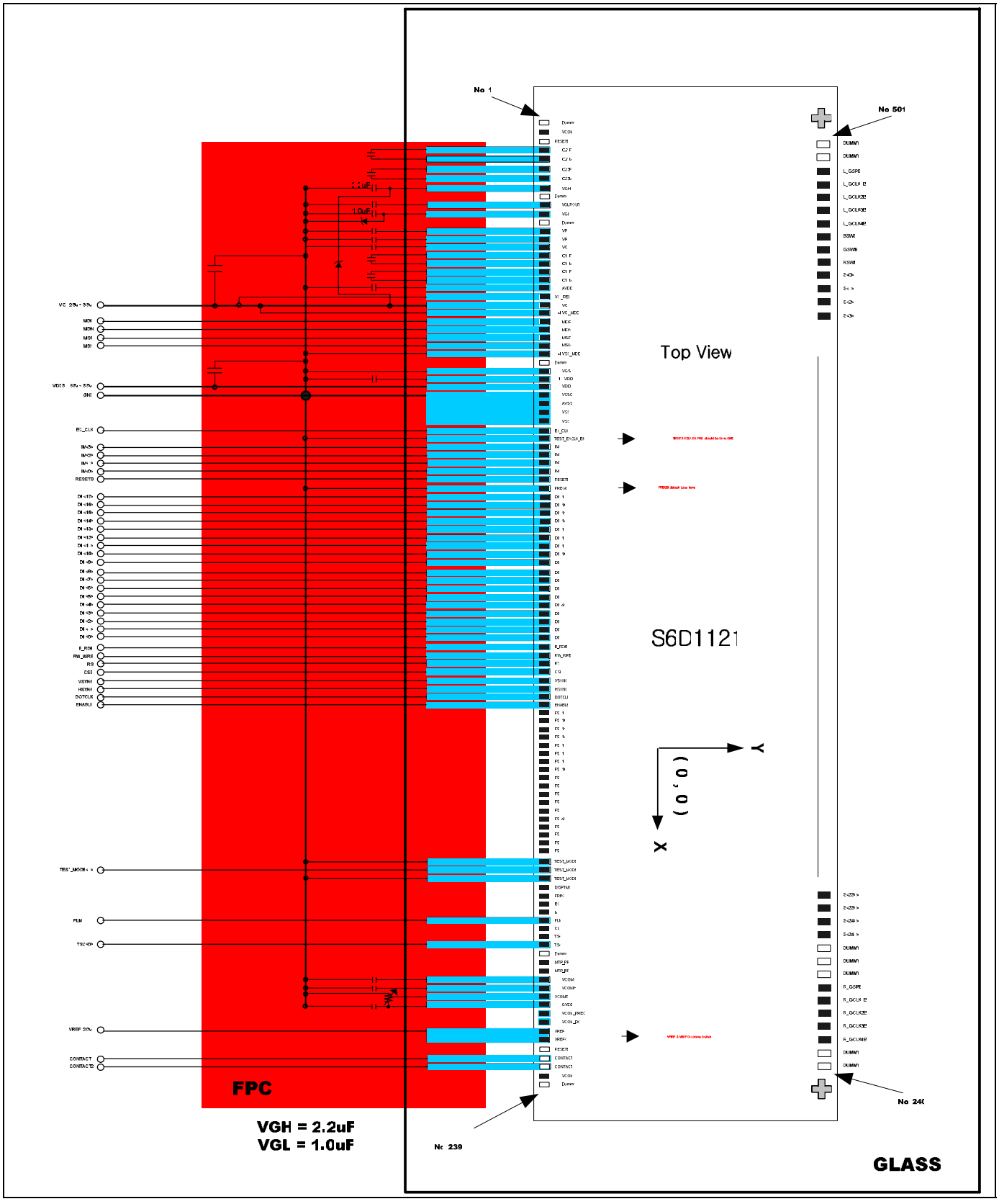
Table 8.9.3 Current Consumption during Setting MTP

Item	Symbol	condition	Min	Typ	Max	Unit
Current consumption during setting MTP	IMTP_EP	MTP_EP = 21.5V	-	-	0.6	mA
	IMTP_PP	MTP_PP = 17.5V	-	-	0.6	

NOTE: simulation result, with common power condition VDD3=2.8V, VDD=1.5V, VCI=2.8V

9. APPLICATIONS

9.1 APPICATION CIRCUIT EXAMPLE



REVISION HISTORY

Date	Contents	Version
Aug. 30, 2006	- Preliminary Version 0.0	Ver. 0.0
Sep. 27. 2006	- Update the Power right and LTPS timing	Ver. 0.1
Oct. 11, 2006	- Update the external power on/off sequence and LTPS timing	Ver. 0.2
Oct. 30, 2006	- Added VSYNC I/F, update LTPS timing (R/G/B multiplexer)	Ver. 0.3
Nov. 24. 2006	- Removed VCL C31M, C31P, - Pin name was changed(MTPD, MTPG, RW_WRB, E_RDB) - Updated the IVDD3,IVCI on STB and SLP mode - MDDI IO DC / AC characteristics - Table 5.2.1.1 Display Operation Mode - 5.2.11.4 MTP sequence flow - Power Control 6 (R15H) (changed VCOMH , VCOMPREC) - Added VCOM_OFF Reg - Table 7.2.9 Function Configuration Table of Direct VCOM Driving and Coupling VCOM Driving Method - Display Control 2 (R08H): back porch ➔ front porch - Initial value of R7AH - Serial Interface Timing Diagram - Removed 2 line interlace partial mode timing diagram - Added 97h register - Removed FUSE ALIGN KEY - Changed Instruction Setup Flow - Changed and added Power OD/OF sequence - Removed AUTO_C reg(R16h)	Ver. 0.31
Dec. 18. 2006	- LTPS timing value of Register changed.(R72H ~ R77H) - VML(4:0) ➔ VML(5:0) : Amplitude of Voltage changed - (R16H) VCOMH Voltage Changed - Removed AMP_AB register (R16H) - Initial value of R16H changed - Confirmed PAD CONFIGURATION - Updated Align Key Configuration - Update PAD Center Coordinates - DC & AC characteristics changed (ILOAD, LCD source driver delay, GATE, MUX) - RESET TIMING was updated - STEP_3 reg. was hidden - Update Application Citcuit Example - Update CPU / RGB / Serial interface AC characteristics - Confirmed Align key configuration and coordinate	Ver. 0.32
Dec. 20. 2006	- Update output voltages range - Update Power Supply Pins Description - Update output voltage amplitude of Gate Driver Control Pins and RGB Switch Control Pins - Update power circuit architecture - Modified Relation between R15h and MTP - Removed 8.7Ltps gate signal level shifter ac characteristics description - Added 8.8 Sub panel signal characteristics - Removed PT = '00' function on using the panel with gate driver.	Ver. 0.33
Dec. 28. 2006	- Changed size of input and output bump	Ver. 0.34
Jan. 08. 2007	- Changed EOR function - Correcting Typo. - Replaced VCOMR register by VCMR register.	Ver. 0.35
Jan. 11. 20067	- 5.2.4 RGB Interface updated - Chanhed AC Timing (tWDS, tWDH, tRDD, tTDH)	Ver. 0.36
Jan. 12. 2007	- The name of odd and even frame changed to 1st, 2nd frame In LCD Driving Waveform Control	

Jan.25. 2007	- removed BT and changed GVD ➔ VRH in set up flow of Power Supply, - VGL ➔ VGLROUT in 126 pages - FMP2-0 ➔ FMP1-0 in 128 pages - VGLROUT values was changed In Power Control 4 (R13H)	
Mar. 07. 2007	- VCOMH = 2.65 x VCOMR In Power Control 6 (R15H): - When R_STP[2:0] = 000 , R Source Output Start Point (R72H) was changed. (4 clocks ➔ 1 clocks) - When G_STP[2:0] = 111, , R Source Output Start Point (R73H) was changed.(Disable ➔ 15clock cycles) - When B_BPW[2:0] = 111, B Mux Start Pulse Width timing cont기(R77H) was changed (15 clock cycles ➔ Disable) - The setup range of VMCHG range was changed .(0 ≤ VMCHG ≤ 3 ➔ 1 ≤ VMCHG ≤ 4) - VCOMR range was added - The function of VCI1_OFF register was changed. And the circuit was added. - FLD function was added on Display Control 1 (R07H) - RGB Interface Timing (VSYNC falling , HSYNC falling) - IVDD3 Current consumption during normal operation was changed from 150 uA to 200uA. - Shorted contacts to VSS. - The Set up Flows of Power Supply were changed. - The VR1C register initial value was changed . - Figure 5.5.4.1 Memory Data Read Sequence was changed. - Figure 5.5.4.2 Memory Data Write Sequence was changed. - Added WINDOW display sequence diagram.	Ver. 0.37
Mar. 09. 2007	- Added PAD size discription and In-chip height description. - Removed VGLROUT in Table 8.2.1 DC Characteristics - Changed Min & Max value of V_{SO} - Modified description of VMA in R15H	Ver. 0.38
Apr. 20. 2007	- In RGB and VSYNC mode, BP + FP must be even value. - Added VGH and VGL Cap. Information.	Ver. 0.39
May. 15. 2007	- AVDD minium voltage changed (4.02 ➔ 3.4) - Corrected errors. - Corrected top block diagram . - Modified Power sequence diagram. - Coupling mode Power Sequence change - VC register table change - Added temperature condition in LCD source driver output voltage range	Ver 0.40
May. 26. 2007	- S6D1121 SPEC 1.00 Version Release.	Ver 1.00

NOTICE

Precautions for Light

When S6D1121 is exposed to light, it may cause motion of electrons inside the semiconductors, which might lead to a change in device characteristics. Hence, the users of the packages who may expose chips to external light such as COB, COG, TCP and COF must consider effective methods to block out light from reaching the IC on all parts of the surface area, the top, bottom and the sides of the chip. Follow the precautions below when using the products.

Consider and verify the penetrating light protection to the IC at substrate (board or glass) or product design stage. Always test and inspect products under the environment with no penetration of light