

2.4-GHz *Bluetooth*[®] low energy System-on-Chip

Check for Samples: [CC2540F128](#), [CC2540F256](#)

FEATURES

- True Single-Chip BLE Solution: CC2540 Can Run Both Application and BLE Protocol Stack, Includes Peripherals to Interface With Wide Range of Sensors, Etc.
- 6-mm × 6-mm Package
- RF
 - *Bluetooth* low energy technology Compatible
 - Excellent Link Budget (up to 97 dB), Enabling Long-Range Applications Without External Front End
 - Accurate Digital Received Signal-Strength Indicator (RSSI)
 - Suitable for Systems Targeting Compliance With Worldwide Radio Frequency Regulations: ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)
- Layout
 - Few External Components
 - Reference Design Provided
 - 6-mm × 6-mm QFN40 Package
- Low Power
 - Active Mode RX Down to 19.6 mA
 - Active Mode TX (–6 dBm): 24 mA
 - Power Mode 1 (3- μ s Wake-Up): 235 μ A
 - Power Mode 2 (Sleep Timer On): 0.9 μ A
 - Power Mode 3 (External Interrupts): 0.4 μ A
 - Wide Supply Voltage Range (2 V–3.6 V)
 - Full RAM and Register Retention in All Power Modes
- [TPS62730](#) Compatible Low Power in Active Mode
 - RX Down to 15.8 mA (3 V Supply)
 - TX (–6 dBm): 18.6 mA (3 V Supply)
- Microcontroller
 - High-Performance and Low-Power 8051 Microcontroller Core
 - In-System-Programmable Flash, 128 KB or 256 KB
 - 8-KB SRAM
- Peripherals
 - 12-Bit ADC with Eight Channels and Configurable Resolution
 - Integrated High-Performance Op-Amp and Ultralow-Power Comparator
 - General-Purpose Timers (One 16-Bit, Two 8-Bit)
 - 21 General-Purpose I/O Pins (19× 4 mA, 2× 20 mA)
 - 32-kHz Sleep Timer With Capture
 - Two Powerful USARTs With Support for Several Serial Protocols
 - Full-Speed USB Interface
 - IR Generation Circuitry
 - Powerful Five-Channel DMA
 - AES Security Coprocessor
 - Battery Monitor and Temperature Sensor
 - Each CC2540 Contains a Unique 48-bit IEEE Address



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SOFTWARE FEATURES

- **Bluetooth v4.0 Compliant Protocol Stack for Single-Mode BLE Solution**
 - Complete Power-Optimized Stack, Including Controller and Host
 - GAP – Central, Peripheral, Observer, or Broadcaster (Including Combination Roles)
 - ATT / GATT – Client and Server
 - SMP – AES-128 Encryption and Decryption
 - L2CAP
 - Sample Applications and Profiles
 - Generic Applications for GAP Central and Peripheral Roles
 - Proximity, Accelerometer, Simple Keys, and Battery GATT Services
 - Multiple Configuration options
 - Single-Chip Configuration, Allowing Application to Run on CC2540
 - Network Processor Interface for Applications Running on an External Microcontroller
 - BTool – Windows PC Application for Evaluation, Development, and Test
- **Development Tools**
 - CC2540 Mini Development Kit
 - SmartRF™ Software
 - Supported by IAR Embedded Workbench™ Software for 8051

DESCRIPTION

The CC2540 is a cost-effective, low-power, true system-on-chip (SoC) for *Bluetooth* low energy applications. It enables robust BLE master or slave nodes to be built with very low total bill-of-material costs. The CC2540 combines an excellent RF transceiver with an industry-standard enhanced 8051 MCU, in-system programmable flash memory, 8-KB RAM, and many other powerful supporting features and peripherals. The CC2540 is suitable for systems where very low power consumption is required. Very low-power sleep modes are available. Short transition times between operating modes further enable low power consumption.

The CC2540 comes in two different versions: CC2540F128/F256, with 128 and 256 KB of flash memory, respectively.

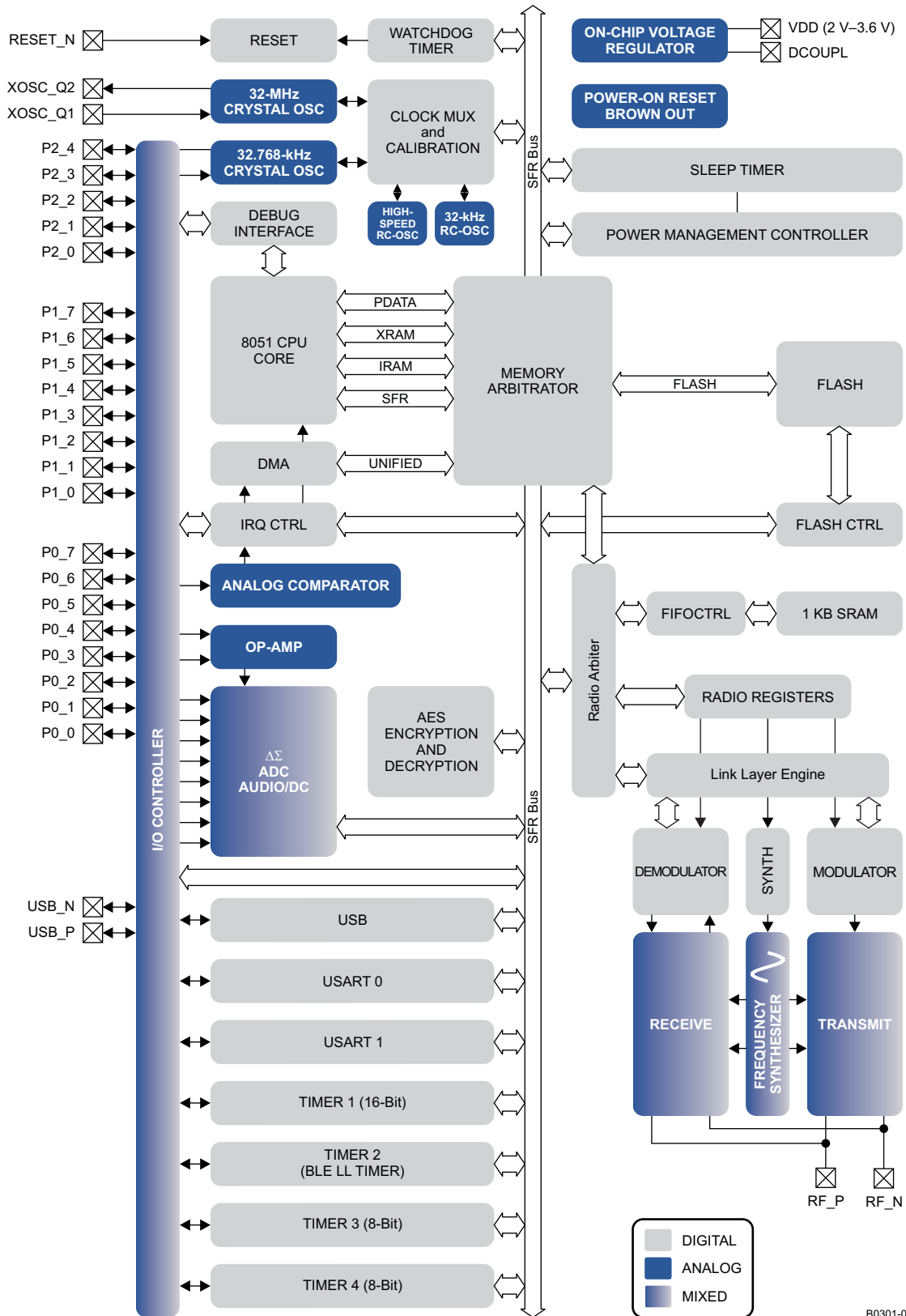
Combined with the *Bluetooth* low energy protocol stack from Texas Instruments, the CC2540F128/F256 forms the market's most flexible and cost-effective single-mode *Bluetooth* low energy solution.

APPLICATIONS

- 2.4-GHz *Bluetooth* low energy Systems
- Mobile Phone Accessories
- Sports and Leisure Equipment
- Consumer Electronics
- Human Interface Devices (Keyboard, Mouse, Remote Control)
- USB Dongles
- Health Care and Medical

CC2540 WITH TPS62730

- **TPS62730** is a 2 MHz Step Down Converter with Bypass Mode
- Extends Battery Lifetime by up to 20%
- Reduced Current in TX and RX
- 30 nA Bypass Mode Current to Support Low Power Modes
- RF Performance Unchanged
- Small Package Allows for Small Solution Size
- CC2540 Controllable



B0301-05



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| | | MIN | MAX | UNIT |
|----------------------------|--|------|---------------------|------|
| Supply voltage | All supply pins must have the same voltage | -0.3 | 3.9 | V |
| Voltage on any digital pin | | -0.3 | VDD + 0.3, ≤ 3.9 | V |
| Input RF level | | | 10 | dBm |
| Storage temperature range | | -40 | 125 | °C |
| ESD ⁽²⁾ | All pads, according to human-body model, JEDEC STD 22, method A114 | | 2 | kV |
| | According to charged-device model, JEDEC STD 22, method C101 | | 750 | V |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) CAUTION: ESD sensitive device. Precautions should be used when handling the device in order to prevent permanent damage.

RECOMMENDED OPERATING CONDITIONS

| | | MIN | MAX | UNIT |
|---|--|-----|-----|------|
| Operating ambient temperature range, T _A | | -40 | 85 | °C |
| Operating supply voltage | | 2 | 3.6 | V |

ELECTRICAL CHARACTERISTICS

Measured on Texas Instruments CC2540 EM reference design with T_A = 25°C and VDD = 3 V

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-----|-----|-----|------|
| I _{core} Core current consumption | Power mode 1. Digital regulator on; 16-MHz RCOSC and 32-MHz crystal oscillator off; 32.768-kHz XOSC, POR, BOD and sleep timer active; RAM and register retention | | 235 | | μA |
| | Power mode 2. Digital regulator off; 16-MHz RCOSC and 32-MHz crystal oscillator off; 32.768-kHz XOSC, POR, and sleep timer active; RAM and register retention | | 0.9 | | |
| | Power mode 3. Digital regulator off; no clocks; POR active; RAM and register retention | | 0.4 | | |
| | Low MCU activity: 32-MHz XOSC running. No radio or peripherals. No flash access, no RAM access. | | 6.7 | | mA |
| I _{peri} Peripheral current consumption (Adds to core current I _{core} for each peripheral unit activated) | Timer 1. Timer running, 32-MHz XOSC used | | 90 | | μA |
| | Timer 2. Timer running, 32-MHz XOSC used | | 90 | | μA |
| | Timer 3. Timer running, 32-MHz XOSC used | | 60 | | μA |
| | Timer 4. Timer running, 32-MHz XOSC used | | 70 | | μA |
| | Sleep timer, including 32.753-kHz RCOSC | | 0.6 | | μA |
| | ADC, when converting | | | 1.2 | |

GENERAL CHARACTERISTICS

 Measured on Texas Instruments CC2540 EM reference design with $T_A = 25^\circ\text{C}$ and $V_{DD} = 3\text{ V}$

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|---|------|-----|------|------|
| WAKE-UP AND TIMING | | | | | |
| Power mode 1 → Active | Digital regulator on, 16-MHz RCOSC and 32-MHz crystal oscillator off. Start-up of 16-MHz RCOSC | | 4 | | μs |
| Power mode 2 or 3 → Active | Digital regulator off, 16-MHz RCOSC and 32-MHz crystal oscillator off. Start-up of regulator and 16-MHz RCOSC | | 120 | | μs |
| Active → TX or RX | Crystal ESR = 16 Ω. Initially running on 16-MHz RCOSC, with 32-MHz XOSC OFF | | 410 | | μs |
| | With 32-MHz XOSC initially on | | 160 | | μs |
| RX/TX turnaround | | | 150 | | μs |
| RADIO PART | | | | | |
| RF frequency range | Programmable in 2-MHz steps | 2402 | | 2480 | MHz |
| Data rate and modulation format | 1 Mbps, GFSK, 250 kHz deviation | | | | |

RF RECEIVE SECTION

 Measured on Texas Instruments CC2540 EM reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3\text{ V}$, $f_c = 2440\text{ MHz}$
1 Mbps, GFSK, 250-kHz deviation, Bluetooth low energy mode, and 0.1% BER⁽¹⁾

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|------|------|-----|------|
| Receiver sensitivity ⁽²⁾ | High-gain mode | | -93 | | dBm |
| Receiver sensitivity ⁽²⁾ | Standard mode | | -87 | | dBm |
| Saturation ⁽³⁾ | | | 6 | | dBm |
| Co-channel rejection ⁽³⁾ | | | -5 | | dB |
| Adjacent-channel rejection ⁽³⁾ | ±1 MHz | | -5 | | dB |
| Alternate-channel rejection ⁽³⁾ | ±2 MHz | | 30 | | dB |
| Blocking ⁽³⁾ | | | -30 | | dBm |
| Frequency error tolerance ⁽⁴⁾ | Including both initial tolerance and drift | -250 | | 250 | kHz |
| Symbol rate error tolerance ⁽⁵⁾ | | -80 | | 80 | ppm |
| Spurious emission. Only largest spurious emission stated within each band. | Conducted measurement with a 50-Ω single-ended load. Complies with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66 | | -75 | | dBm |
| Current consumption | RX mode, standard mode, no peripherals active, low MCU activity, MCU at 250 kHz | | 19.6 | | mA |
| | RX mode, high-gain mode, no peripherals active, low MCU activity, MCU at 250 kHz | | 22.1 | | |

(1) 0.1% BER maps to 30.8% PER

(2) The receiver sensitivity setting is programmable using a TI BLE stack vendor-specific API command. The default value is standard mode.

(3) Results based on standard gain mode

(4) Difference between center frequency of the received RF signal and local oscillator frequency

(5) Difference between incoming symbol rate and the internally generated symbol rate

RF TRANSMIT SECTION

Measured on Texas Instruments CC2540 EM reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3\text{ V}$ and $f_c = 2440\text{ MHz}$

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|--|-----|----------|-----|----------|
| Output power | Delivered to a single-ended 50- Ω load through a balun using maximum recommended output power setting | | 4 | | dBm |
| | Delivered to a single-ended 50- Ω load through a balun using minimum recommended output power setting | | -23 | | |
| Programmable output power range | Delivered to a single-ended 50 Ω load through a balun | | 27 | | dB |
| Spurious emissions | Conducted measurement with a 50- Ω single-ended load. Complies with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66 ⁽¹⁾ | | -41 | | dBm |
| Current consumption | TX mode, -23-dBm output power, no peripherals active, low MCU activity, MCU at 250 kHz | | 21.1 | | mA |
| | TX mode, -6-dBm output power, no peripherals active, low MCU activity, MCU at 250 kHz | | 23.8 | | |
| | TX mode, 0-dBm output power, no peripherals active, low MCU activity, MCU at 250 kHz | | 27 | | |
| | TX mode, 4-dBm output power, no peripherals active, low MCU activity, MCU at 250 kHz | | 31.6 | | |
| Optimum load impedance | Differential impedance as seen from the RF port (RF_P and RF_N) toward the antenna | | 70 + j30 | | Ω |

(1) Designs with antenna connectors that require conducted ETSI compliance at 64 MHz should insert an LC resonator in front of the antenna connector. Use a 1.6-nH inductor in parallel with a 1.8-pF capacitor. Connect both from the signal trace to a good RF ground.

CURRENT CONSUMPTION WITH TPS62730

Measured on Texas Instruments CC2540TPS62730 EM reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3\text{ V}$, and $f_c = 2440\text{ MHz}$.

1 Mbps, GFSK, 250 kHz deviation, Bluetooth™ low energy mode, 1% BER⁽¹⁾

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|--|-----|------|-----|------|
| Current Consumption | RX mode, standard mode, no peripherals active, low MCU activity, MCU at 1 MHz | | 15.8 | | mA |
| | RX mode, high-gain mode, no peripherals active, low MCU activity, MCU at 1 MHz | | 17.8 | | |
| | TX mode, -23 dBm output power, no peripherals active, low MCU activity, MCU at 1 MHz | | 16.5 | | |
| | TX mode, -6 dBm output power, no peripherals active, low MCU activity, MCU at 1 MHz | | 18.6 | | |
| | TX mode, 0 dBm output power, no peripherals active, low MCU activity, MCU at 1 MHz | | 21 | | |
| | TX mode, 4 dBm output power, no peripherals active, low MCU activity, MCU at 1 MHz | | 24.6 | | |

(1) 0.1% BER maps to 30.8% PER

32-MHz CRYSTAL OSCILLATOR

 Measured on Texas Instruments CC2540 EM reference design with $T_A = 25^\circ\text{C}$ and $V_{DD} = 3\text{ V}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|------------------------------|--|-----|------|-----|----------|
| Crystal frequency | | | | 32 | | MHz |
| Crystal frequency accuracy requirement ⁽¹⁾ | | | -40 | | 40 | ppm |
| ESR | Equivalent series resistance | | 6 | | 60 | Ω |
| C_0 | Crystal shunt capacitance | | 1 | | 7 | pF |
| C_L | Crystal load capacitance | | 10 | | 16 | pF |
| Start-up time | | | | 0.25 | | ms |
| Power-down guard time | | The crystal oscillator must be in power down for a guard time before it is used again. This requirement is valid for all modes of operation. The need for power-down guard time can vary with crystal type and load. | 3 | | | ms |

(1) Including aging and temperature dependency, as specified by [1]

32.768-kHz CRYSTAL OSCILLATOR

 Measured on Texas Instruments CC2540 EM reference design with $T_A = 25^\circ\text{C}$ and $V_{DD} = 3\text{ V}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|------------------------------|-----------------|-----|--------|-----|------------|
| Crystal frequency | | | | 32.768 | | kHz |
| Crystal frequency accuracy requirement ⁽¹⁾ | | | -40 | | 40 | ppm |
| ESR | Equivalent series resistance | | | 40 | 130 | k Ω |
| C_0 | Crystal shunt capacitance | | | 0.9 | 2 | pF |
| C_L | Crystal load capacitance | | | 12 | 16 | pF |
| Start-up time | | | | 0.4 | | s |

(1) Including aging and temperature dependency, as specified by [1]

32-kHz RC OSCILLATOR

 Measured on Texas Instruments CC2540 EM reference design with $T_w = 25^\circ\text{C}$ and $V_{DD} = 3\text{ V}$.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-----------------|-----|-------------|-----|---------------------|
| Calibrated frequency ⁽¹⁾ | | | 32.753 | | kHz |
| Frequency accuracy after calibration | | | $\pm 0.2\%$ | | |
| Temperature coefficient ⁽²⁾ | | | 0.4 | | $\%/^\circ\text{C}$ |
| Supply-voltage coefficient ⁽³⁾ | | | 3 | | $\%/V$ |
| Calibration time ⁽⁴⁾ | | | 2 | | ms |

(1) The calibrated 32-kHz RC oscillator frequency is the 32-MHz XTAL frequency divided by 977.

(2) Frequency drift when temperature changes after calibration

(3) Frequency drift when supply voltage changes after calibration

(4) When the 32-kHz RC oscillator is enabled, it is calibrated when a switch from the 16-MHz RC oscillator to the 32-MHz crystal oscillator is performed while SLEPCMD.OSC32K_CALDIS is set to 0.

16-MHz RC OSCILLATOR

Measured on Texas Instruments CC2540 EM reference design with $T_A = 25^\circ\text{C}$ and $VDD = 3\text{ V}$

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-----------------|-----|-------|-----|------|
| Frequency ⁽¹⁾ | | | 16 | | MHz |
| Uncalibrated frequency accuracy | | | ±18% | | |
| Calibrated frequency accuracy | | | ±0.6% | | |
| Start-up time | | | 10 | | µs |
| Initial calibration time ⁽²⁾ | | | 50 | | µs |

(1) The calibrated 16-MHz RC oscillator frequency is the 32-MHz XTAL frequency divided by 2.

(2) When the 16-MHz RC oscillator is enabled, it is calibrated when a switch from the 16-MHz RC oscillator to the 32-MHz crystal oscillator is performed while SLEEP_CMD.OSC_PD is set to 0.

RSSI CHARACTERISTICS

Measured on Texas Instruments CC2540 EM reference design with $T_A = 25^\circ\text{C}$ and $VDD = 3\text{ V}$

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------|-----|-----|-----|------|
| Useful RSSI range ⁽¹⁾ | High-gain mode | -99 | -44 | | dBm |
| | Standard mode | -90 | -35 | | |
| Absolute uncalibrated RSSI accuracy ⁽¹⁾ | High-gain mode | | ±4 | | dB |
| Step size (LSB value) | | | 1 | | dB |

(1) Assuming CC2540 EM reference design. Other RF designs give an offset from the reported value.

FREQUENCY SYNTHESIZER CHARACTERISTICS

Measured on Texas Instruments CC2540 EM reference design with $T_A = 25^\circ\text{C}$, $VDD = 3\text{ V}$ and $f_c = 2440\text{ MHz}$

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------|-------------------------------|-----|------|-----|--------|
| Phase noise, unmodulated carrier | At ±1-MHz offset from carrier | | -109 | | dBc/Hz |
| | At ±3-MHz offset from carrier | | -112 | | |
| | At ±5-MHz offset from carrier | | -119 | | |

ANALOG TEMPERATURE SENSOR

Measured on Texas Instruments CC2540 EM reference design with $T_A = 25^\circ\text{C}$ and $VDD = 3\text{ V}$

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|--------------------------------------|--|-----|------|-----|--------|--------|
| Output | Measured using integrated ADC, internal band-gap voltage reference, and maximum resolution | | 1480 | | 12-bit | |
| Temperature coefficient | | | 4.5 | | /1°C | |
| Voltage coefficient | | | | 1 | | /0.1 V |
| Initial accuracy without calibration | | | | ±10 | | °C |
| Accuracy using 1-point calibration | | | | ±5 | | °C |
| Current consumption when enabled | | | | 0.5 | | mA |

OP-AMP CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{DD} = 3\text{ V}$, . All measurement results are obtained using the CC2540 reference designs post-calibration.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-------------------------------------|-----|----------------|-----|--------------------------------|
| Chopping Configuration, Register APCFG = 0x07, OPAMPMC = 0x03, OPAMPC = 0x01 | | | | | |
| Output maximum voltage | | | $V_{DD} - 0.1$ | | V |
| Output minimum voltage | | | 0.1 | | V |
| Open-loop gain | | | 108 | | dB |
| Gain-bandwidth product | | | 2 | | MHz |
| Slew rate | | | 2.6 | | V/ μs |
| Input maximum voltage | | | V_{DD} | | V |
| Input minimum voltage | | | 0 | | mV |
| Input offset voltage | | | 40 | | μV |
| CMRR Common-mode rejection ratio | | | 90 | | dB |
| Supply current | | | 0.4 | | mA |
| Input noise voltage | $f = 0.01\text{ Hz to }1\text{ Hz}$ | | 1.1 | | $\text{nV}/\sqrt{(\text{Hz})}$ |
| | $f = 0.1\text{ Hz to }10\text{ Hz}$ | | 1.7 | | |
| Non-Chopping Configuration, Register APCFG = 0x07, OPAMPMC = 0x00, OPAMPC = 0x01 | | | | | |
| Output maximum voltage | | | $V_{DD} - 0.1$ | | V |
| Output minimum voltage | | | 0.1 | | V |
| Open-loop gain | | | 108 | | dB |
| Gain-bandwidth product | | | 2 | | MHz |
| Slew rate | | | 2.6 | | V/ μs |
| Input maximum voltage | | | V_{DD} | | V |
| Input minimum voltage | | | 0 | | mV |
| Input offset voltage | | | 3.2 | | mV |
| CMRR Common-mode rejection ratio | | | 90 | | dB |
| Supply current | | | 0.4 | | mA |
| Input noise voltage | $f = 0.01\text{ Hz to }1\text{ Hz}$ | | 60 | | $\text{nV}/\sqrt{(\text{Hz})}$ |
| | $f = 0.1\text{ Hz to }10\text{ Hz}$ | | 65 | | |

COMPARATOR CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{DD} = 3\text{ V}$. All measurement results are obtained using the CC2540 reference designs, post-calibration.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------|-----------------|-----|----------|-----|------------------------------|
| Common-mode maximum voltage | | | V_{DD} | | V |
| Common-mode minimum voltage | | | -0.3 | | |
| Input offset voltage | | | 1 | | mV |
| Offset vs temperature | | | 16 | | $\mu\text{V}/^\circ\text{C}$ |
| Offset vs operating voltage | | | 4 | | mV/V |
| Supply current | | | 230 | | nA |
| Hysteresis | | | 0.15 | | mV |

ADC CHARACTERISTICS

T_A = 25°C and VDD = 3 V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|---|--|-----|-------|-----|------|
| | Input voltage | VDD is voltage on AVDD5 pin | 0 | | VDD | V |
| | External reference voltage | VDD is voltage on AVDD5 pin | 0 | | VDD | V |
| | External reference voltage differential | VDD is voltage on AVDD5 pin | 0 | | VDD | V |
| | Input resistance, signal | Simulated using 4-MHz clock speed | | 197 | | kΩ |
| | Full-scale signal ⁽¹⁾ | Peak-to-peak, defines 0 dBFS | | 2.97 | | V |
| ENOB ⁽¹⁾ | Effective number of bits | Single-ended input, 7-bit setting | | 5.7 | | bits |
| | | Single-ended input, 9-bit setting | | 7.5 | | |
| | | Single-ended input, 10-bit setting | | 9.3 | | |
| | | Single-ended input, 12-bit setting | | 10.3 | | |
| | | Differential input, 7-bit setting | | 6.5 | | |
| | | Differential input, 9-bit setting | | 8.3 | | |
| | | Differential input, 10-bit setting | | 10 | | |
| | | Differential input, 12-bit setting | | 11.5 | | |
| | | 10-bit setting, clocked by RCOSC | | 9.7 | | |
| | | 12-bit setting, clocked by RCOSC | | 10.9 | | |
| | Useful power bandwidth | 7-bit setting, both single and differential | | 0–20 | | kHz |
| THD | Total harmonic distortion | Single ended input, 12-bit setting, –6 dBFS ⁽¹⁾ | | –75.2 | | dB |
| | | Differential input, 12-bit setting, –6 dBFS ⁽¹⁾ | | –86.6 | | |
| | Signal to nonharmonic ratio | Single-ended input, 12-bit setting ⁽¹⁾ | | 70.2 | | dB |
| | | Differential input, 12-bit setting ⁽¹⁾ | | 79.3 | | |
| | | Single-ended input, 12-bit setting, –6 dBFS ⁽¹⁾ | | 78.8 | | |
| | | Differential input, 12-bit setting, –6 dBFS ⁽¹⁾ | | 88.9 | | |
| CMRR | Common-mode rejection ratio | Differential input, 12-bit setting, 1-kHz sine (0 dBFS), limited by ADC resolution | | >84 | | dB |
| | Crosstalk | Single ended input, 12-bit setting, 1-kHz sine (0 dBFS), limited by ADC resolution | | >84 | | dB |
| | Offset | Midscale | | –3 | | mV |
| | Gain error | | | 0.68% | | |
| DNL | Differential nonlinearity | 12-bit setting, mean ⁽¹⁾ | | 0.05 | | LSB |
| | | 12-bit setting, maximum ⁽¹⁾ | | 0.9 | | |
| INL | Integral nonlinearity | 12-bit setting, mean ⁽¹⁾ | | 4.6 | | LSB |
| | | 12-bit setting, maximum ⁽¹⁾ | | 13.3 | | |
| | | 12-bit setting, mean, clocked by RCOSC | | 10 | | |
| | | 12-bit setting, max, clocked by RCOSC | | 29 | | |
| | | | | | | |
| SINAD (–THD+N) | Signal-to-noise-and-distortion | Single ended input, 7-bit setting ⁽¹⁾ | | 35.4 | | dB |
| | | Single ended input, 9-bit setting ⁽¹⁾ | | 46.8 | | |
| | | Single ended input, 10-bit setting ⁽¹⁾ | | 57.5 | | |
| | | Single ended input, 12-bit setting ⁽¹⁾ | | 66.6 | | |
| | | Differential input, 7-bit setting ⁽¹⁾ | | 40.7 | | |
| | | Differential input, 9-bit setting ⁽¹⁾ | | 51.6 | | |
| | | Differential input, 10-bit setting ⁽¹⁾ | | 61.8 | | |
| | | Differential input, 12-bit setting ⁽¹⁾ | | 70.8 | | |

(1) Measured with 300-Hz sine-wave input and VDD as reference.

ADC CHARACTERISTICS (continued)

T_A = 25°C and VDD = 3 V

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------|-----|------|-----|---------|
| Conversion time | 7-bit setting | | 20 | | μs |
| | 9-bit setting | | 36 | | |
| | 10-bit setting | | 68 | | |
| | 12-bit setting | | 132 | | |
| Power consumption | | | 1.2 | | mA |
| Internal reference VDD coefficient | | | 4 | | mV/V |
| Internal reference temperature coefficient | | | 0.4 | | mV/10°C |
| Internal reference voltage | | | 1.24 | | V |

CONTROL INPUT AC CHARACTERISTICS

T_A = -40°C to 85°C, VDD = 2 V to 3.6 V.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|-----|-----|-----|------|
| System clock, f _{SYSCLK} t _{SYSCLK} = 1/ f _{SYSCLK} | The undivided system clock is 32 MHz when crystal oscillator is used. The undivided system clock is 16 MHz when calibrated 16-MHz RC oscillator is used. | 16 | | 32 | MHz |
| RESET_N low duration | See item 1, Figure 1. This is the shortest pulse that is recognized as a complete reset pin request. Note that shorter pulses may be recognized but do not lead to complete reset of all modules within the chip. | 1 | | | μs |
| Interrupt pulse duration | See item 2, Figure 1. This is the shortest pulse that is recognized as an interrupt request. | 20 | | | ns |

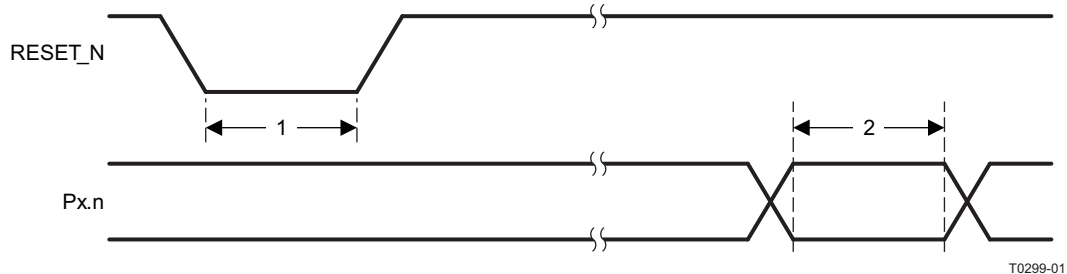
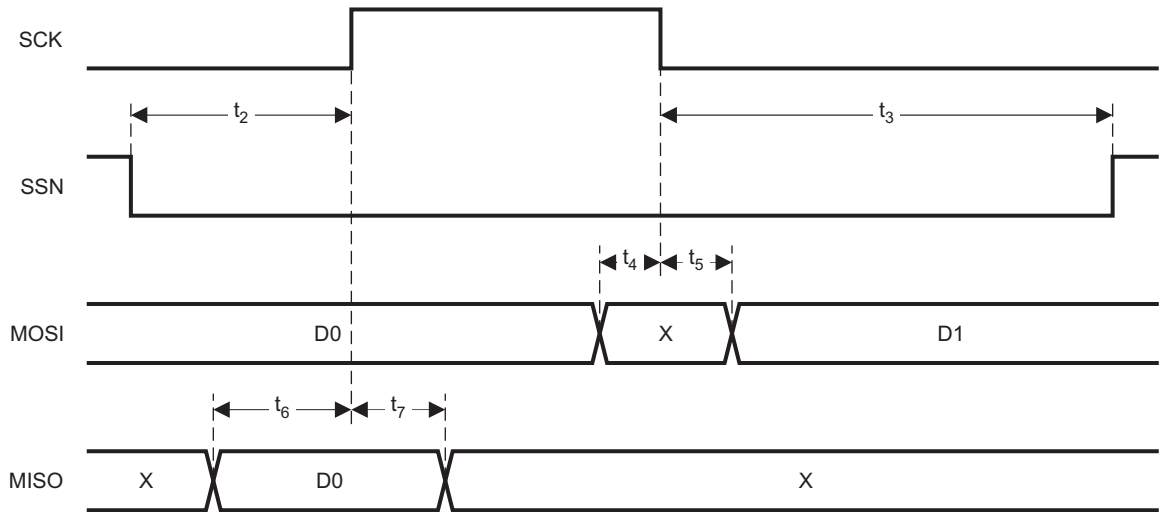


Figure 1. Control Input AC Characteristics

SPI AC CHARACTERISTICS

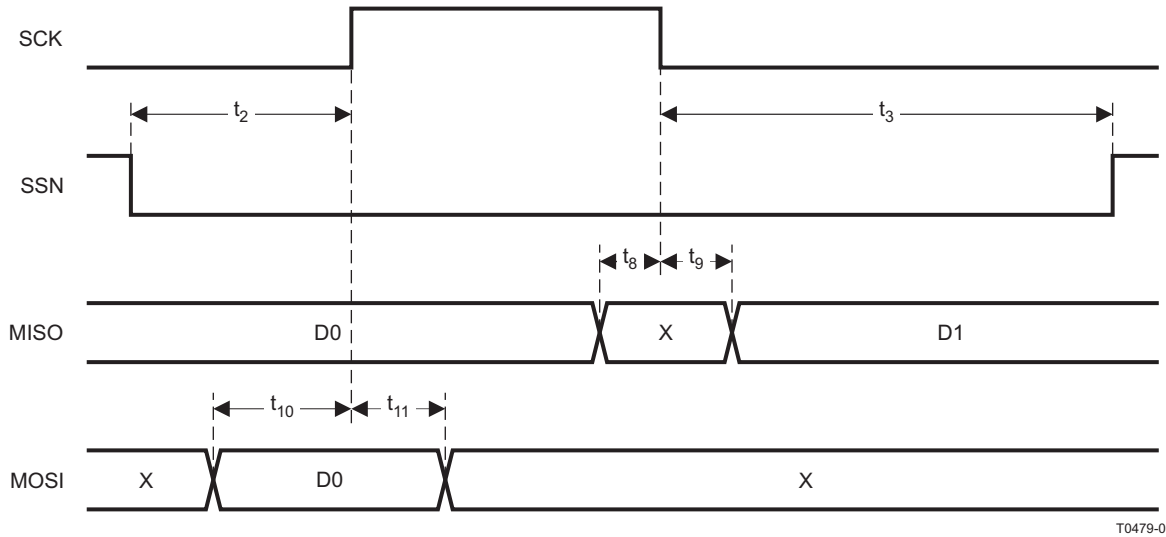
T_A = -40°C to 85°C, VDD = 2 V to 3.6 V

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------|----------------------|-----|-----|-----|------|
| t ₁ SCK period | Master, RX and TX | 250 | | | ns |
| | Slave, RX and TX | 250 | | | |
| SCK duty cycle | Master | | 50% | | |
| t ₂ SSN low to SCK | Master | 63 | | | ns |
| | Slave | 63 | | | |
| t ₃ SCK to SSN high | Master | 63 | | | ns |
| | Slave | 63 | | | |
| t ₄ MOSI early out | Master, load = 10 pF | | | 7 | ns |
| t ₅ MOSI late out | Master, load = 10 pF | | | 10 | ns |
| t ₆ MISO setup | Master | 90 | | | ns |
| t ₇ MISO hold | Master | 10 | | | ns |
| SCK duty cycle | Slave | | 50% | | ns |
| t ₁₀ MOSI setup | Slave | 35 | | | ns |
| t ₁₁ MOSI hold | Slave | 10 | | | ns |
| t ₉ MISO late out | Slave, load = 10 pF | | | 95 | ns |
| Operating frequency | Master, TX only | | | 8 | MHz |
| | Master, RX and TX | | | 4 | |
| | Slave, RX only | | | 8 | |
| | Slave, RX and TX | | | 4 | |



T0478-01

Figure 2. SPI Master AC Characteristics



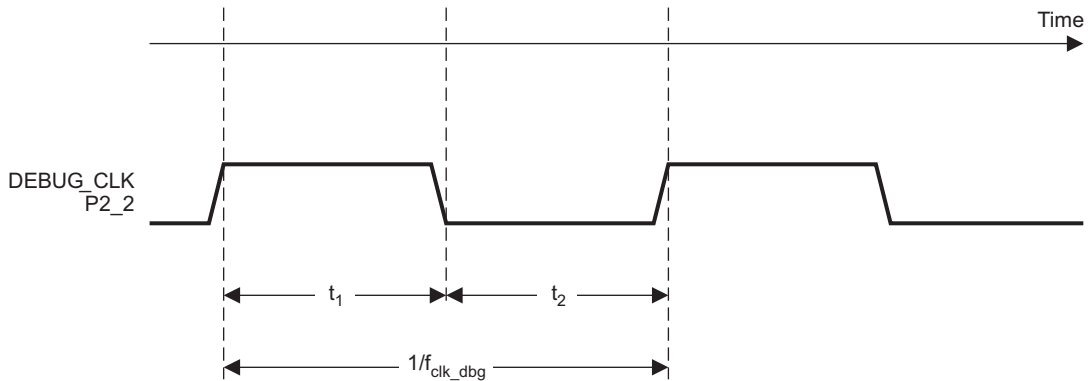
T0479-01

Figure 3. SPI Slave AC Characteristics

DEBUG INTERFACE AC CHARACTERISTICS

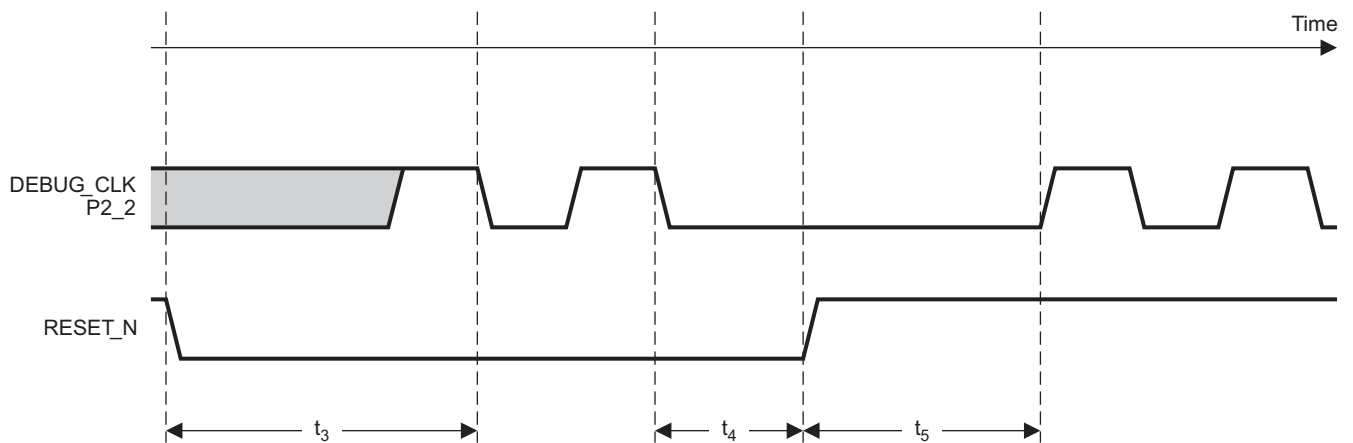
T_A = -40°C to 85°C, VDD = 2 V to 3.6 V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|---|-----------------|-----|-----|-----|------|
| f _{clk_dbg} | Debug clock frequency (see Figure 4) | | | | 12 | MHz |
| t ₁ | Allowed high pulse on clock (see Figure 4) | | 35 | | | ns |
| t ₂ | Allowed low pulse on clock (see Figure 4) | | 35 | | | ns |
| t ₃ | EXT_RESET_N low to first falling edge on debug clock (see Figure 6) | | 167 | | | ns |
| t ₄ | Falling edge on clock to EXT_RESET_N high (see Figure 6) | | 83 | | | ns |
| t ₅ | EXT_RESET_N high to first debug command (see Figure 6) | | 83 | | | ns |
| t ₆ | Debug data setup (see Figure 5) | | 2 | | | ns |
| t ₇ | Debug data hold (see Figure 5) | | 4 | | | ns |
| t ₈ | Clock-to-data delay (see Figure 5) | Load = 10 pF | | | 30 | ns |



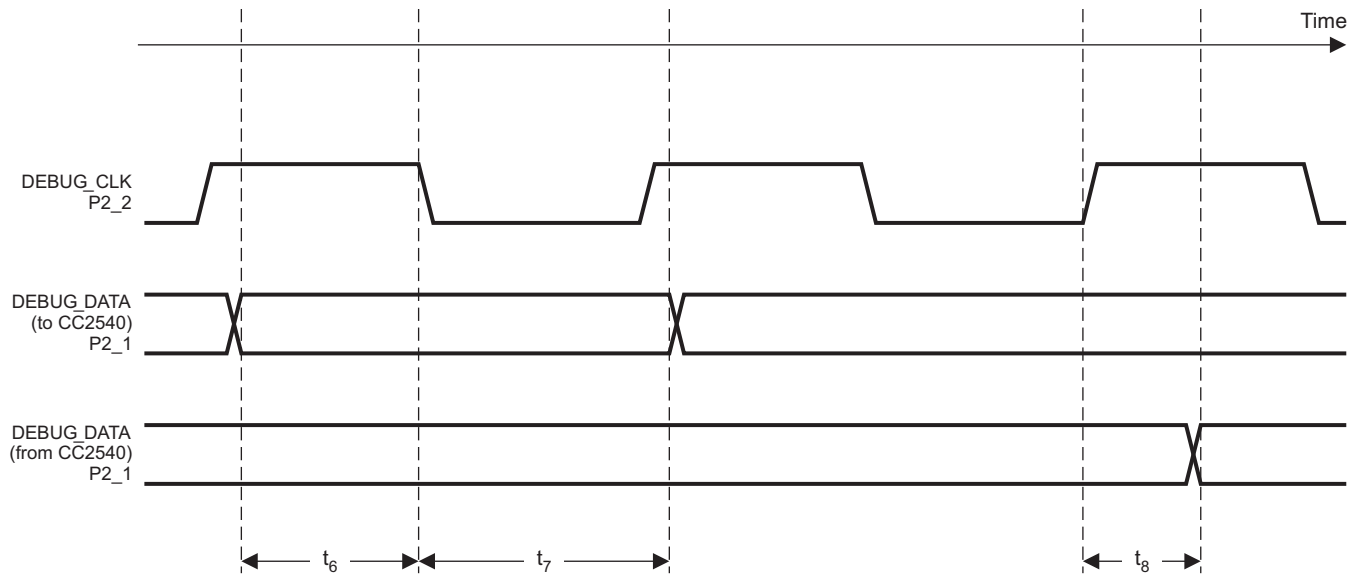
T0436-01

Figure 4. Debug Clock – Basic Timing



T0437-01

Figure 5. Debug Enable Timing



T0438-02

Figure 6. Data Setup and Hold Timing

TIMER INPUTS AC CHARACTERISTICS

$T_A = -40^{\circ}\text{C}$ to 85°C , $V_{DD} = 2\text{ V}$ to 3.6 V

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|---|-----|-----|-----|---------------------|
| Input capture pulse duration | Synchronizers determine the shortest input pulse that can be recognized. The synchronizers operate at the current system clock rate (16 MHz or 32 MHz). | 1.5 | | | t_{SYSCLK} |

DC CHARACTERISTICS

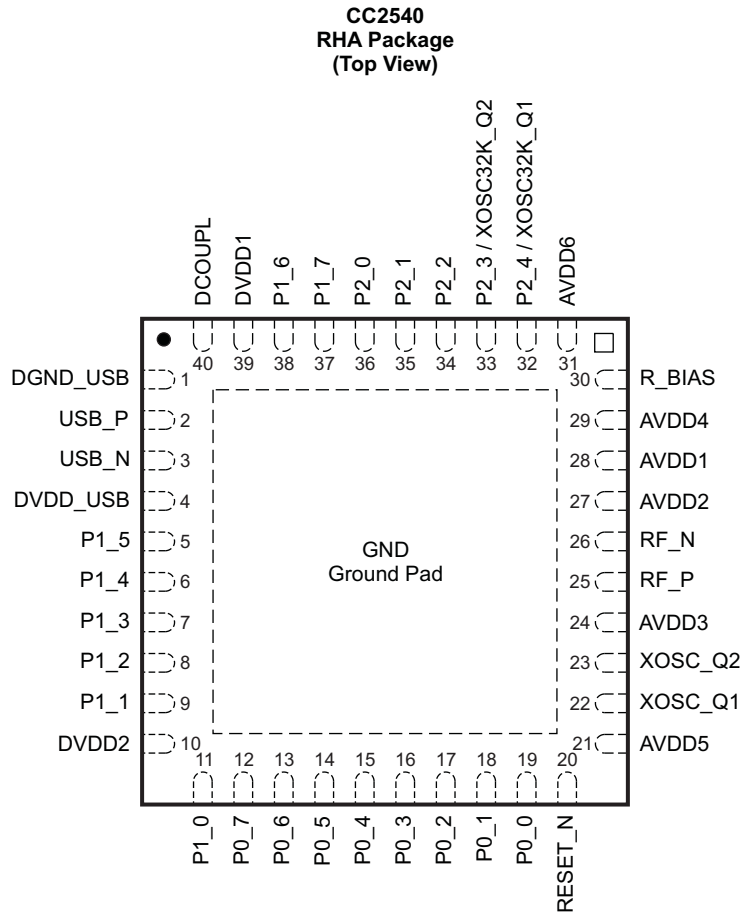
$T_A = 25^{\circ}\text{C}$, $V_{DD} = 3\text{ V}$

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------------|------------------|-----|-----|-----|------------|
| Logic-0 input voltage | | | | 0.5 | V |
| Logic-1 input voltage | | 2.5 | | | V |
| Logic-0 input current | Input equals 0 V | -50 | | 50 | nA |
| Logic-1 input current | Input equals VDD | -50 | | 50 | nA |
| I/O-pin pullup and pulldown resistors | | | 20 | | k Ω |
| Logic-0 output voltage, 4- mA pins | Output load 4 mA | | | 0.5 | V |
| Logic-1 output voltage, 4-mA pins | Output load 4 mA | 2.4 | | | V |

DEVICE INFORMATION

PIN DESCRIPTIONS

The CC2540 pinout is shown in [Figure 7](#) and a short description of the pins follows.



P0076-05

NOTE: The exposed ground pad must be connected to a solid ground plane, as this is the ground connection for the chip.

Figure 7. Pinout Top View

PIN DESCRIPTIONS

| PIN NAME | PIN | PIN TYPE | DESCRIPTION |
|---------------------|-----|----------------------------|--|
| AVDD1 | 28 | Power (analog) | 2-V–3.6-V analog power-supply connection |
| AVDD2 | 27 | Power (analog) | 2-V–3.6-V analog power-supply connection |
| AVDD3 | 24 | Power (analog) | 2-V–3.6-V analog power-supply connection |
| AVDD4 | 29 | Power (analog) | 2-V–3.6-V analog power-supply connection |
| AVDD5 | 21 | Power (analog) | 2-V–3.6-V analog power-supply connection |
| AVDD6 | 31 | Power (analog) | 2-V–3.6-V analog power-supply connection |
| DCOUPPL | 40 | Power (digital) | 1.8-V digital power-supply decoupling. Do not use for supplying external circuits. |
| DGND_USB | 1 | Ground pin | Connect to GND |
| DVDD_USB | 4 | Power (digital) | 2-V–3.6-V digital power-supply connection |
| DVDD1 | 39 | Power (digital) | 2-V–3.6-V digital power-supply connection |
| DVDD2 | 10 | Power (digital) | 2-V–3.6-V digital power-supply connection |
| GND | — | Ground | The ground pad must be connected to a solid ground plane. |
| P0_0 | 19 | Digital I/O | Port 0.0 |
| P0_1 | 18 | Digital I/O | Port 0.1 |
| P0_2 | 17 | Digital I/O | Port 0.2 |
| P0_3 | 16 | Digital I/O | Port 0.3 |
| P0_4 | 15 | Digital I/O | Port 0.4 |
| P0_5 | 14 | Digital I/O | Port 0.5 |
| P0_6 | 13 | Digital I/O | Port 0.6 |
| P0_7 | 12 | Digital I/O | Port 0.7 |
| P1_0 | 11 | Digital I/O | Port 1.0 – 20-mA drive capability |
| P1_1 | 9 | Digital I/O | Port 1.1 – 20-mA drive capability |
| P1_2 | 8 | Digital I/O | Port 1.2 |
| P1_3 | 7 | Digital I/O | Port 1.3 |
| P1_4 | 6 | Digital I/O | Port 1.4 |
| P1_5 | 5 | Digital I/O | Port 1.5 |
| P1_6 | 38 | Digital I/O | Port 1.6 |
| P1_7 | 37 | Digital I/O | Port 1.7 |
| P2_0 | 36 | Digital I/O | Port 2.0 |
| P2_1 | 35 | Digital I/O | Port 2.1 |
| P2_2 | 34 | Digital I/O | Port 2.2 |
| P2_3/ XOSC32K_Q2 | 33 | Digital I/O, Analog I/O | Port 2.3/32.768 kHz XOSC |
| P2_4/ XOSC32K_Q1 | 32 | Digital I/O, Analog I/O | Port 2.4/32.768 kHz XOSC |
| RBIAS | 30 | Analog I/O | External precision bias resistor for reference current |
| RESET_N | 20 | Digital input | Reset, active-low |
| RF_N | 26 | RF I/O | Negative RF input signal to LNA during RX Negative RF output signal from PA during TX |
| RF_P | 25 | RF I/O | Positive RF input signal to LNA during RX Positive RF output signal from PA during TX |
| USB_N | 3 | Digital I/O | USB N |
| USB_P | 2 | Digital I/O | USB P |
| XOSC_Q1 | 22 | Analog I/O | 32-MHz crystal oscillator pin 1 or external-clock input |
| XOSC_Q2 | 23 | Analog I/O | 32-MHz crystal oscillator pin 2 |

BLOCK DIAGRAM

A block diagram of the CC2540 is shown in Figure 8. The modules can be roughly divided into one of three categories: CPU-related modules; modules related to power, test, and clock distribution; and radio-related modules. In the following subsections, a short description of each module is given.

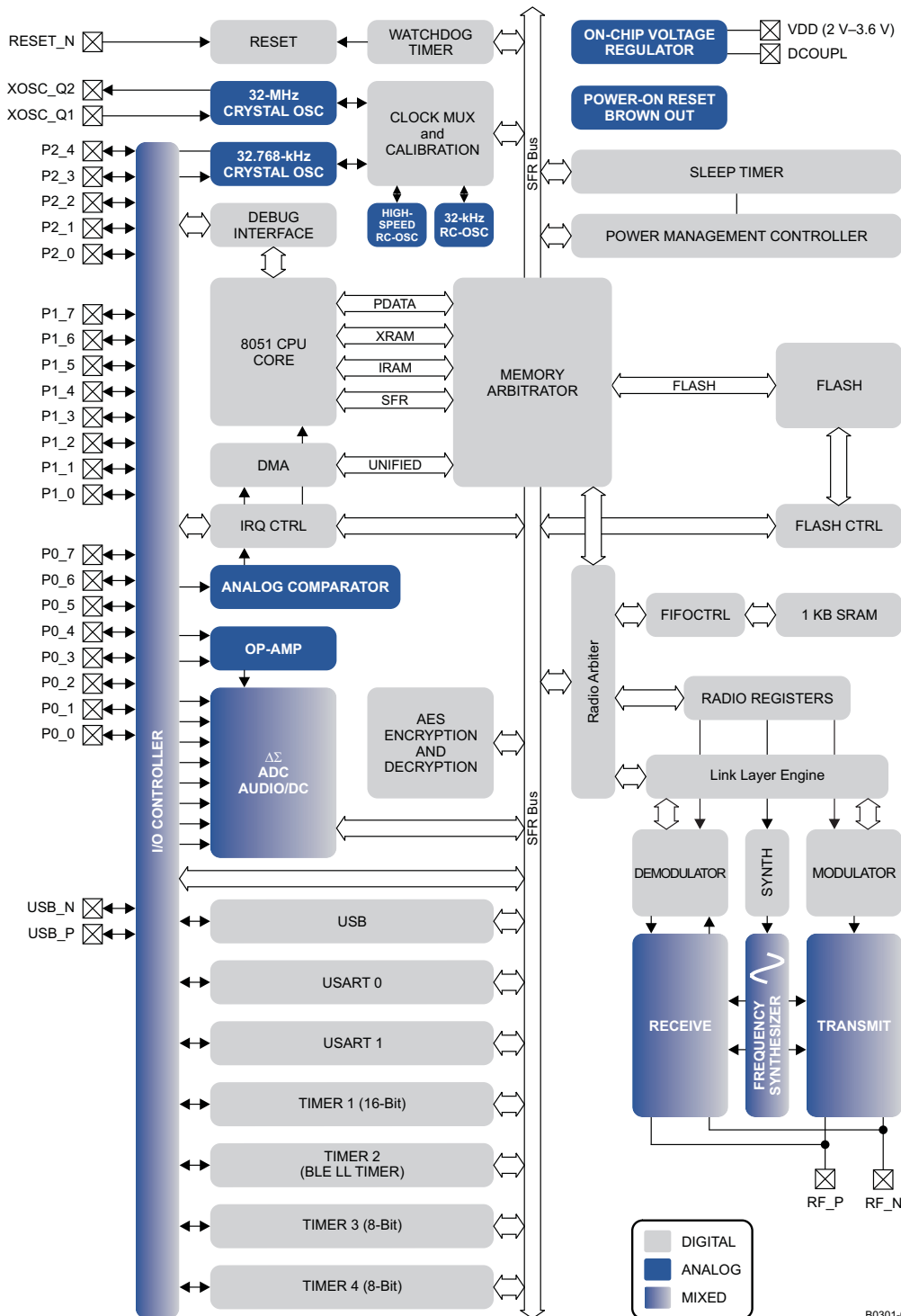


Figure 8. CC2540 Block Diagram

BLOCK DESCRIPTIONS

CPU and Memory

The **8051 CPU core** is a single-cycle 8051-compatible core. It has three different memory access busses (SFR, DATA, and CODE/XDATA), a debug interface, and an 18-input extended interrupt unit.

The **memory arbiter** is at the heart of the system, as it connects the CPU and DMA controller with the physical memories and all peripherals through the SFR bus. The memory arbiter has four memory-access points, access of which can map to one of three physical memories: an SRAM, flash memory, and XREG/SFR registers. It is responsible for performing arbitration and sequencing between simultaneous memory accesses to the same physical memory.

The **SFR bus** is drawn conceptually in [Figure 8](#) as a common bus that connects all hardware peripherals to the memory arbiter. The SFR bus in the block diagram also provides access to the radio registers in the radio register bank, even though these are indeed mapped into XDATA memory space.

The **8-KB SRAM** maps to the DATA memory space and to parts of the XDATA memory spaces. The SRAM is an ultralow-power SRAM that retains its contents even when the digital part is powered off (power modes 2 and 3).

The **128/256 KB flash block** provides in-circuit programmable non-volatile program memory for the device, and maps into the CODE and XDATA memory spaces.

Peripherals

Writing to the flash block is performed through a **flash controller** that allows page-wise erasure and 4-bytewise programming. See User Guide for details on the flash controller.

A versatile five-channel **DMA controller** is available in the system, accesses memory using the XDATA memory space, and thus has access to all physical memories. Each channel (trigger, priority, transfer mode, addressing mode, source and destination pointers, and transfer count) is configured with DMA descriptors that can be located anywhere in memory. Many of the hardware peripherals (AES core, flash controller, USARTs, timers, ADC interface, etc.) can be used with the DMA controller for efficient operation by performing data transfers between a single SFR or XREG address and flash/SRAM.

Each CC2540 contains a unique 48-bit IEEE address that can be used as the public device address for a *Bluetooth* device. Designers are free to use this address, or provide their own, as described in the *Bluetooth* specification.

The **interrupt controller** services a total of 18 interrupt sources, divided into six interrupt groups, each of which is associated with one of four interrupt priorities. I/O and sleep timer interrupt requests are serviced even if the device is in a sleep mode (power modes 1 and 2) by bringing the CC2540 back to the active mode.

The **debug interface** implements a proprietary two-wire serial interface that is used for in-circuit debugging. Through this debug interface, it is possible to erase or program the entire flash memory, control which oscillators are enabled, stop and start execution of the user program, execute instructions on the 8051 core, set code breakpoints, and single-step through instructions in the code. Using these techniques, it is possible to perform in-circuit debugging and external flash programming elegantly.

The **I/O controller** is responsible for all general-purpose I/O pins. The CPU can configure whether peripheral modules control certain pins or whether they are under software control, and if so, whether each pin is configured as an input or output and if a pullup or pulldown resistor in the pad is connected. Each peripheral that connects to the I/O pins can choose between two different I/O pin locations to ensure flexibility in various applications.

The **sleep timer** is an ultralow-power timer that can either use an external 32.768-kHz crystal oscillator or an internal 32.753-kHz RC oscillator. The sleep timer runs continuously in all operating modes except power mode 3. Typical applications of this timer are as a real-time counter or as a wake-up timer to get out of power modes 1 or 2.

A built-in **watchdog timer** allows the CC2540 to reset itself if the firmware hangs. When enabled by software, the watchdog timer must be cleared periodically; otherwise, it resets the device when it times out.

Timer 1 is a 16-bit timer with timer/counter/PWM functionality. It has a programmable prescaler, a 16-bit period value, and five individually programmable counter/capture channels, each with a 16-bit compare value. Each of the counter/capture channels can be used as a PWM output or to capture the timing of edges on input signals. It can also be configured in IR generation mode, where it counts timer 3 periods and the output is ANDed with the output of timer 3 to generate modulated consumer IR signals with minimal CPU interaction.

Timer 2 is a 40-bit timer used by the *Bluetooth* low energy stack. It has a 16-bit counter with a configurable timer period and a 24-bit overflow counter that can be used to keep track of the number of periods that have transpired. A 40-bit capture register is also used to record the exact time at which a start-of-frame delimiter is received/transmitted or the exact time at which transmission ends. There are two 16-bit timer-compare registers and two 24-bit overflow-compare registers that can be used to give exact timing for start of RX or TX to the radio or general interrupts.

Timer 3 and timer 4 are 8-bit timers with timer/counter/PWM functionality. They have a programmable prescaler, an 8-bit period value, and one programmable counter channel with an 8-bit compare value. Each of the counter channels can be used as PWM output.

USART 0 and USART 1 are each configurable as either an SPI master/slave or a UART. They provide double buffering on both RX and TX and hardware flow control and are thus well suited to high-throughput full-duplex applications. Each USART has its own high-precision baud-rate generator, thus leaving the ordinary timers free for other uses. When configured as SPI slaves, the USARTs sample the input signal using SCK directly instead of using some oversampling scheme, and are thus well-suited for high data rates.

The **AES encryption/decryption core** allows the user to encrypt and decrypt data using the AES algorithm with 128-bit keys. The AES core also supports ECB, CBC, CFB, OFB, CTR, and CBC-MAC, as well as hardware support for CCM.

The **ADC** supports 7 to 12 bits of resolution with a corresponding range of bandwidths from 30-kHz to 4-kHz, respectively. DC and audio conversions with up to eight input channels (I/O controller pins) are possible. The inputs can be selected as single-ended or differential. The reference voltage can be internal, AVDD, or a single-ended or differential external signal. The ADC also has a temperature-sensor input channel. The ADC can automate the process of periodic sampling or conversion over a sequence of channels.

The **operational amplifier** is intended to provide front-end buffering and gain for the ADC. Both inputs as well as the output are available on pins, so the feedback network is fully customizable. A chopper-stabilized mode is available for applications that need good accuracy with high gain.

The ultralow-power **analog comparator** enables applications to wake up from PM2 or PM3 based on an analog signal. Both inputs are brought out to pins; the reference voltage must be provided externally. The comparator output is connected to the I/O controller interrupt detector and can be treated by the MCU as a regular I/O pin interrupt.

TYPICAL CHARACTERISTICS

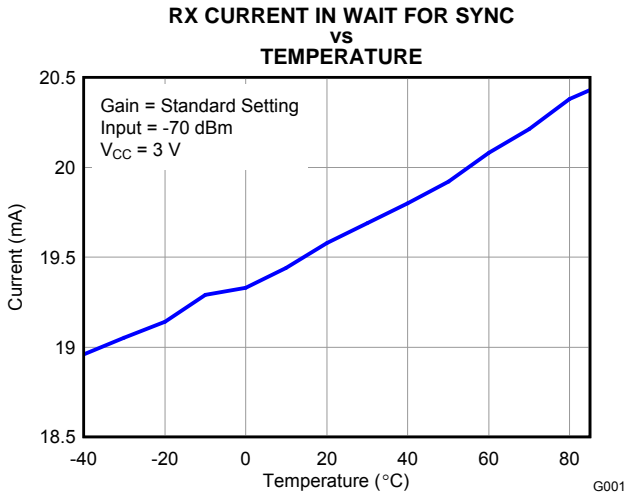


Figure 9.

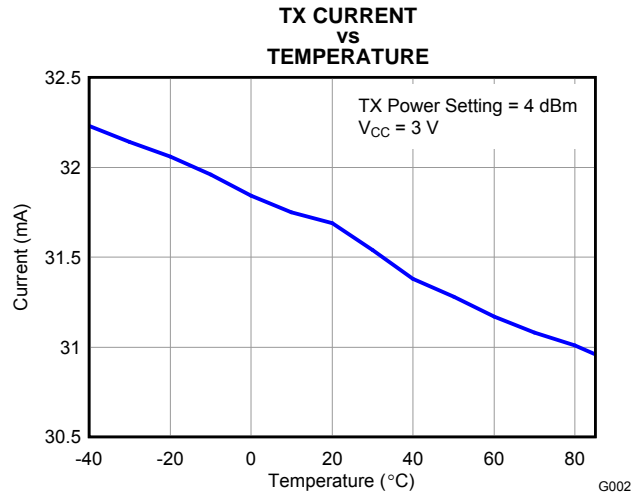


Figure 10.

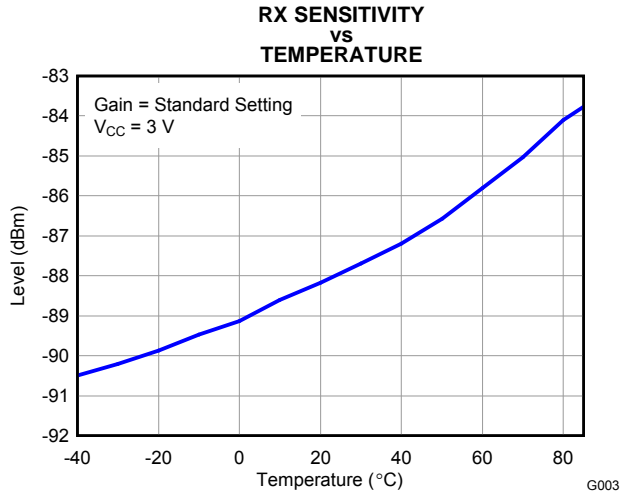


Figure 11.

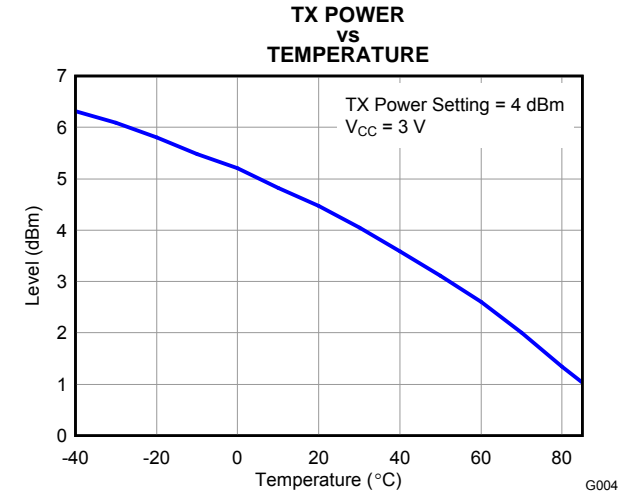


Figure 12.

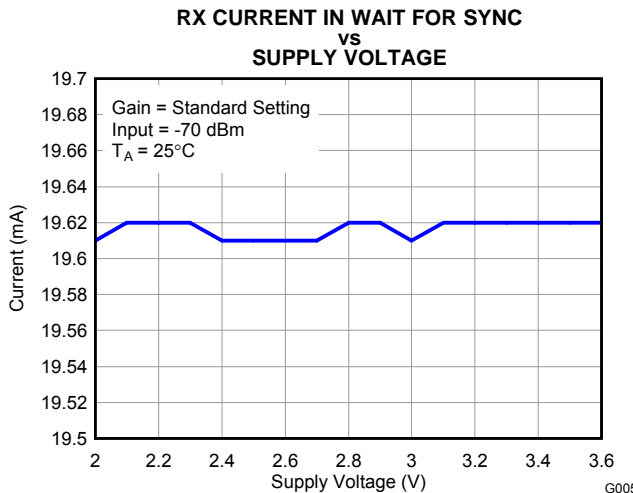


Figure 13.

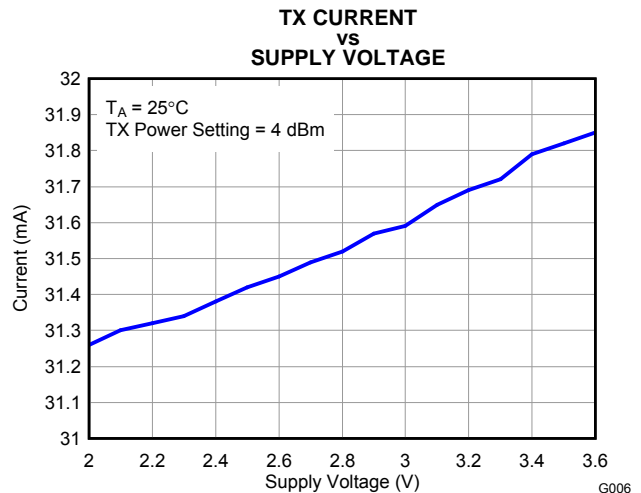


Figure 14.

TYPICAL CHARACTERISTICS (continued)

**RX SENSITIVITY
vs
SUPPLY VOLTAGE**

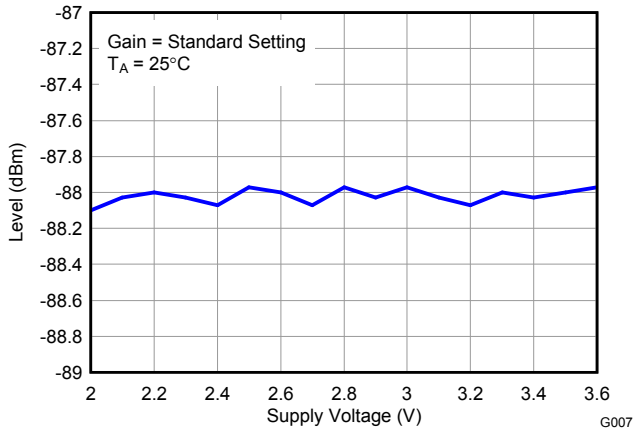


Figure 15.

**TX POWER
vs
SUPPLY VOLTAGE**

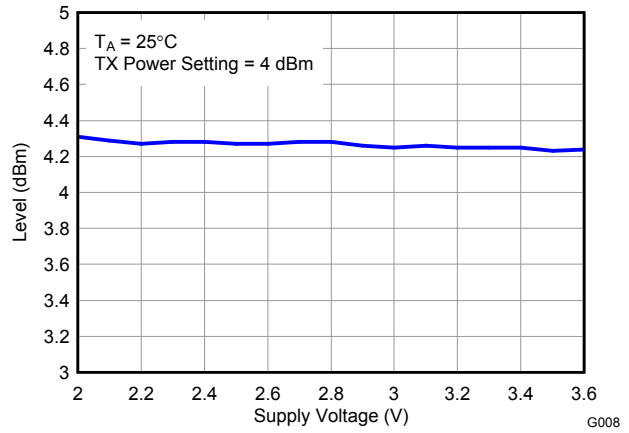


Figure 16.

**RX SENSITIVITY
vs
FREQUENCY**

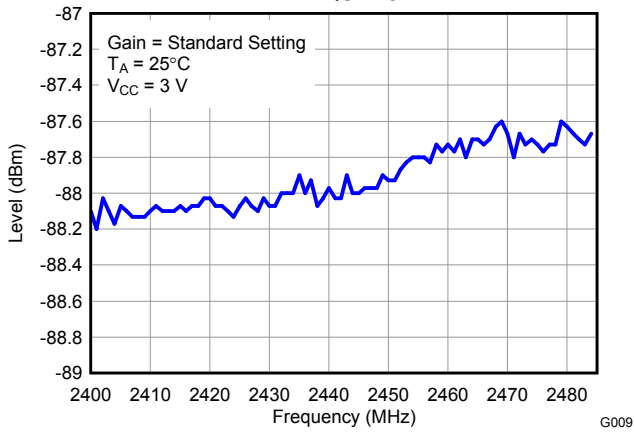


Figure 17.

**RX INTERFERER REJECTION (SELECTIVITY)
vs
INTERFERER FREQUENCY**

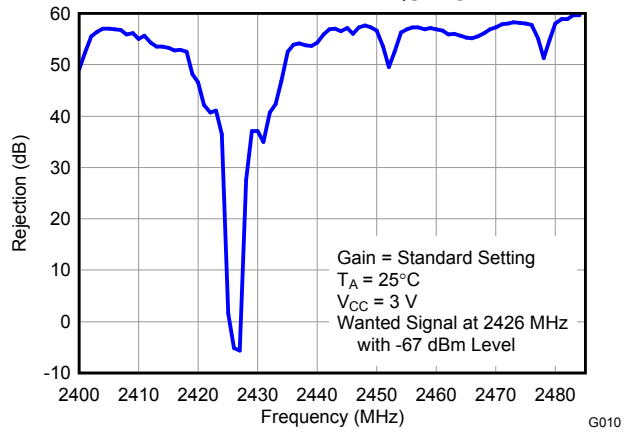


Figure 18.

**TX POWER
vs
FREQUENCY**

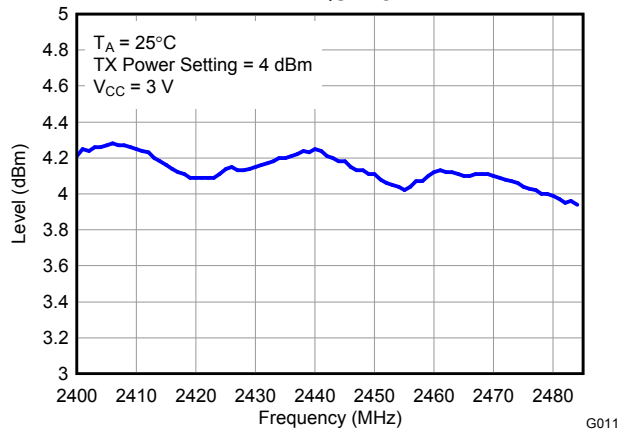


Figure 19.

TYPICAL CHARACTERISTICS (continued)
Table 1. Output Power and Current Consumption⁽¹⁾⁽²⁾

| Typical Output Power (dBm) | Typical Current Consumption (mA) | Typical Current Consumption With TPS62730 (mA) |
|----------------------------|----------------------------------|--|
| 4 | 32 | 24.6 |
| 0 | 27 | 21 |
| -6 | 24 | 18.5 |
| -23 | 21 | 16.5 |

- (1) Measured on Texas Instruments CC2540 EM reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3\text{ V}$ and $f_c = 2440\text{ MHz}$. See [SWRU191](#) for recommended register settings
- (2) Measured on Texas Instruments CC2540TPS62730 EM reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3\text{ V}$ and $f_c = 2440\text{ MHz}$. See [SWRU191](#) for recommended register settings

TYPICAL CURRENT SAVINGS

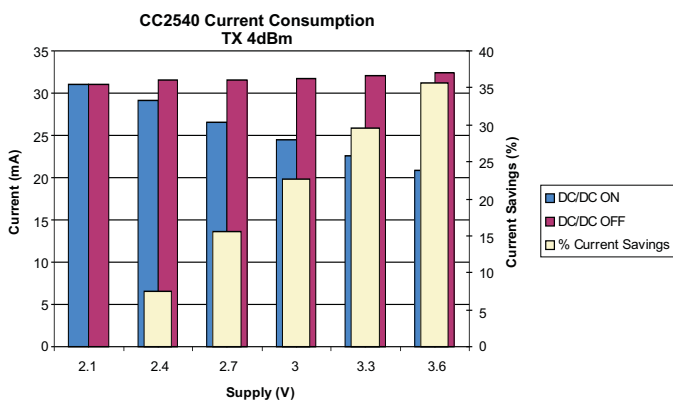


Figure 20. Current Savings in TX at Room Temperature

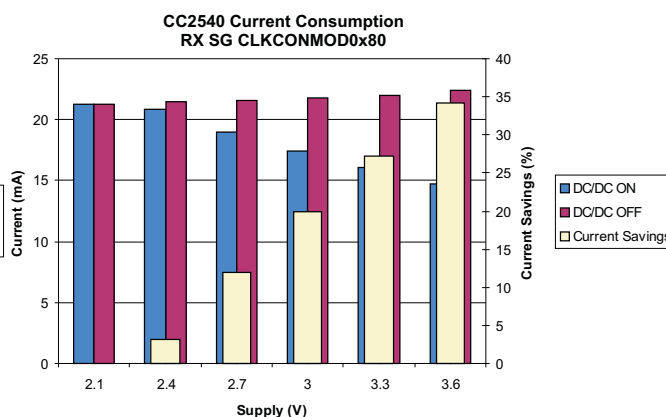
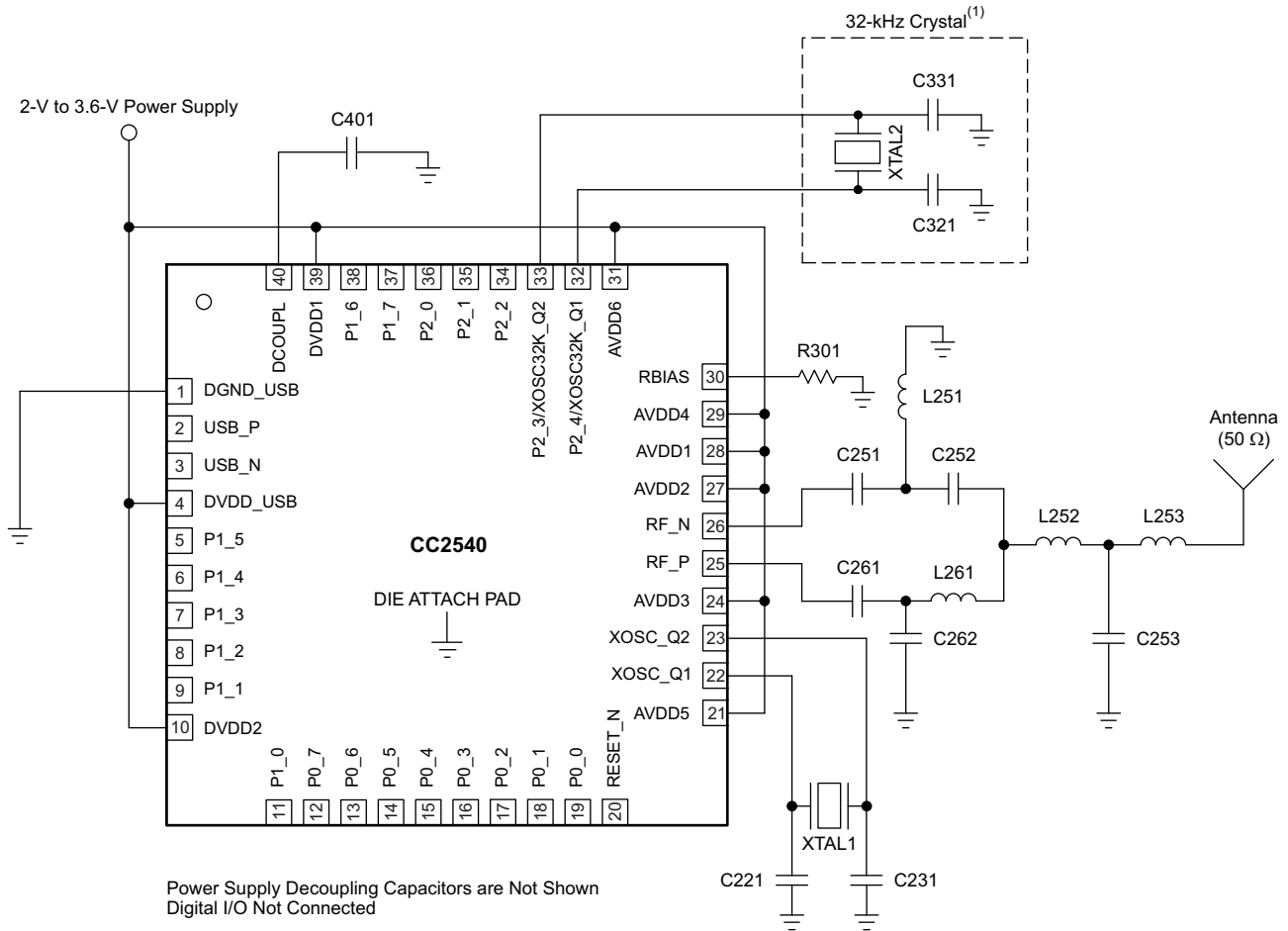


Figure 21. Current Savings in RX at Room Temperature

The application note ([SWRA365](#)) has information regarding the CC2540 and TPS62730 como board and the current savings that can be achieved using the como board.

APPLICATION INFORMATION

Few external components are required for the operation of the CC2540. A typical application circuit is shown in Figure 22.



Power Supply Decoupling Capacitors are Not Shown
Digital I/O Not Connected

S0383-03

(1) 32-kHz crystal is mandatory when running the chip in low-power modes, except if the link layer is in the standby state (Vol. 6 Part B Section 1.1 in [1]).

NOTE: Different antenna alternatives will be provided as reference designs.

Figure 22. CC2540 Application Circuit

Table 2. Overview of External Components (Excluding Supply Decoupling Capacitors)

| Component | Description | Value |
|-----------|---------------------------------|-------|
| C221 | 32-MHz xtal loading capacitor | 12 pF |
| C231 | 32-MHz xtal loading capacitor | 12 pF |
| C251 | Part of the RF matching network | 18 pF |
| C252 | Part of the RF matching network | 1 pF |
| C253 | Part of the RF matching network | 1 pF |
| C261 | Part of the RF matching network | 18 pF |
| C262 | Part of the RF matching network | 1 pF |
| C321 | 32-kHz xtal loading capacitor | 15 pF |
| C331 | 32-kHz xtal loading capacitor | 15 pF |

Table 2. Overview of External Components (Excluding Supply Decoupling Capacitors) (continued)

| Component | Description | Value |
|-----------|---|---------------|
| C401 | Decoupling capacitor for the internal digital regulator | 1 μ F |
| L251 | Part of the RF matching network | 2 nH |
| L252 | Part of the RF matching network | 1 nH |
| L253 | Part of the RF matching network | 3 nH |
| L261 | Part of the RF matching network | 2 nH |
| R301 | Resistor used for internal biasing | 56 k Ω |

Input/Output Matching

When using an unbalanced antenna such as a monopole, a balun should be used to optimize performance. The balun can be implemented using low-cost discrete inductors and capacitors. The recommended balun shown consists of C262, L261, C252, and L252.

Crystal

An external 32-MHz crystal, XTAL1, with two loading capacitors (C221 and C231) is used for the 32-MHz crystal oscillator. See [32-MHz CRYSTAL OSCILLATOR](#) for details. The load capacitance seen by the 32-MHz crystal is given by:

$$C_L = \frac{1}{\frac{1}{C_{221}} + \frac{1}{C_{231}}} + C_{\text{parasitic}} \quad (1)$$

XTAL2 is an optional 32.768-kHz crystal, with two loading capacitors (C321 and C331) used for the 32.768-kHz crystal oscillator. The 32.768-kHz crystal oscillator is used in applications where both very low sleep-current consumption and accurate wake-up times are needed. The load capacitance seen by the 32.768-kHz crystal is given by:

$$C_L = \frac{1}{\frac{1}{C_{321}} + \frac{1}{C_{331}}} + C_{\text{parasitic}} \quad (2)$$

A series resistor may be used to comply with the ESR requirement.

On-Chip 1.8-V Voltage Regulator Decoupling

The 1.8-V on-chip voltage regulator supplies the 1.8-V digital logic. This regulator requires a decoupling capacitor (C401) for stable operation.

Power-Supply Decoupling and Filtering

Proper power-supply decoupling must be used for optimum performance. The placement and size of the decoupling capacitors and the power supply filtering are very important to achieve the best performance in an application. TI provides a compact reference design that should be followed very closely.

References

1. *Bluetooth*® Core Technical Specification document, version 4.0
http://www.bluetooth.com/SiteCollectionDocuments/Core_V40.zip
2. CC253x System-on-Chip Solution for 2.4-GHz IEEE 802.15.4 and ZigBee® Applications/CC2540 System-on-Chip Solution for 2.4-GHz *Bluetooth* low energy Applications ([SWRU191](#))
3. Current Savings in CC254x Using the TPS62730 ([SWRA365](#))

Additional Information

Texas Instruments offers a wide selection of cost-effective, low-power RF solutions for proprietary and standard-based wireless applications for use in industrial and consumer applications. Our selection includes RF transceivers, RF transmitters, RF front ends, and System-on-Chips as well as various software solutions for the sub-1- and 2.4-GHz frequency bands.

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REVISION HISTORY

| Changes from Revision Original (October 2010) to Revision A | Page |
|--|-------------|
| • Changed several items in Features list | 1 |
| • Changed upper limit of storage temperature range | 4 |
| • Changed ESD rating for charged-device model | 4 |
| • Changed adjacent-channel rejection from 5 dB to –5 dB | 5 |
| Changes from Revision A (May 2011) to Revision B | Page |
| • Added the TPS62730 Compatible Features List | 1 |
| • Added the CC2540 WITH TPS62730 Applications | 2 |
| • Added CURRENT CONSUMPTION WITH TPS62730 characteristics | 6 |
| • Changed Table 1 | 23 |
| • Added the TYPICAL CURRENT SAVINGS section | 23 |
| Changes from Revision B (July 2011) to Revision C | Page |
| • Changed on page 2, under CC2540...item 2 from Application Run Time to Battery Lifetime | 2 |
| • Corrected block diagram | 3 |
| • In the OP-AMP CHARACTERISTICS table, changed several values in the TYP column | 9 |
| Changes from Revision C (November 2011) to Revision D | Page |
| • Changed the Temperature coefficient Unit value From: mV/°C To: / 0.1°C | 8 |
| • Changed Figure 22 text From: Optional 32-kHz Crystal To: 32-kHz Crystal | 24 |
| Changes from Revision D (August 2012) to Revision E | Page |
| • Changed the "Internal reference voltage" TYP value From 1.15 V To: 1.24 V | 11 |
| Changes from Revision E (November 2012) to Revision F | Page |
| • Changed the RF TRANSMIT SECTION, Output power TYP value From: –20 To: –23 | 6 |
| • Changed the RF TRANSMIT SECTION, Programmable output power range TYP value From: 24 To: 27 | 6 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| CC2540F128RHAR | ACTIVE | VQFN | RHA | 40 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | CC2540 F128 | Samples |
| CC2540F128RHAT | ACTIVE | VQFN | RHA | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | CC2540 F128 | Samples |
| CC2540F256RHAR | ACTIVE | VQFN | RHA | 40 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | CC2540 F256 | Samples |
| CC2540F256RHAT | ACTIVE | VQFN | RHA | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | CC2540 F256 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CC2540F128RHAR | VQFN | RHA | 40 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.5 | 12.0 | 16.0 | Q2 |
| CC2540F128RHAT | VQFN | RHA | 40 | 250 | 180.0 | 16.4 | 6.3 | 6.3 | 1.5 | 12.0 | 16.0 | Q2 |
| CC2540F256RHAR | VQFN | RHA | 40 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.5 | 12.0 | 16.0 | Q2 |
| CC2540F256RHAT | VQFN | RHA | 40 | 250 | 180.0 | 16.4 | 6.3 | 6.3 | 1.5 | 12.0 | 16.0 | Q2 |

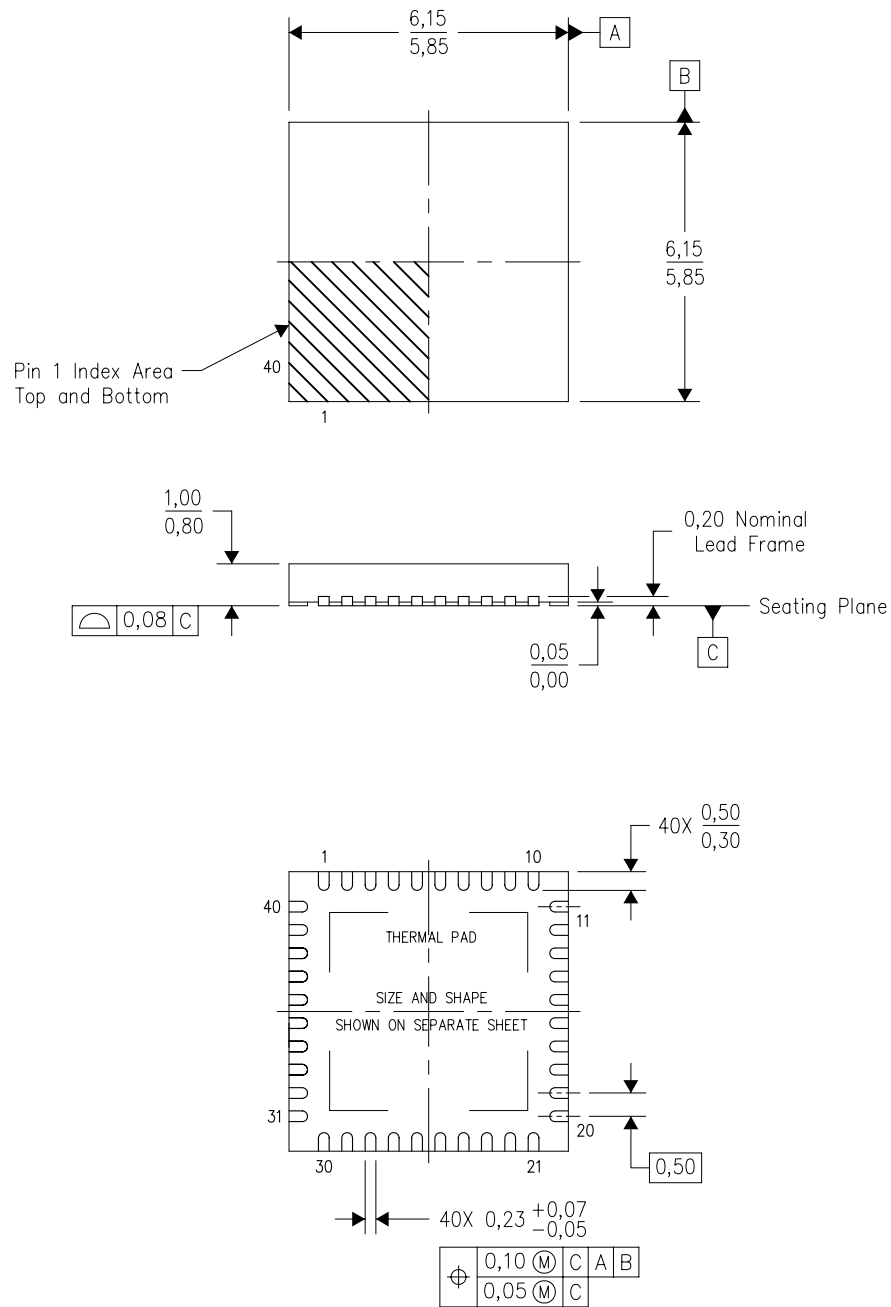
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CC2540F128RHAR | VQFN | RHA | 40 | 2500 | 336.6 | 336.6 | 28.6 |
| CC2540F128RHAT | VQFN | RHA | 40 | 250 | 213.0 | 191.0 | 55.0 |
| CC2540F256RHAR | VQFN | RHA | 40 | 2500 | 336.6 | 336.6 | 28.6 |
| CC2540F256RHAT | VQFN | RHA | 40 | 250 | 213.0 | 191.0 | 55.0 |

RHA (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



Bottom View

4204276/E 06/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) Package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Package complies to JEDEC MO-220 variation VJJD-2.

THERMAL PAD MECHANICAL DATA

RHA (S-PVQFN-N40)

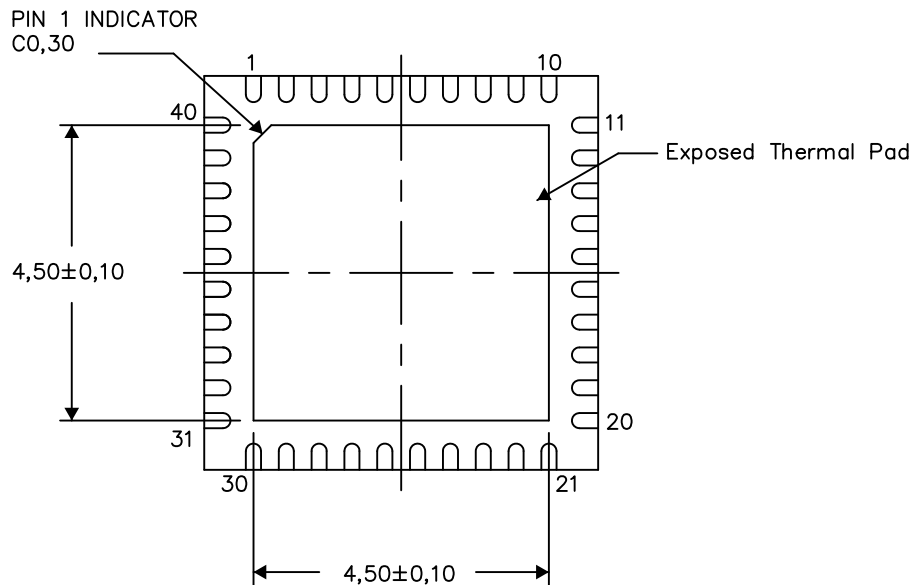
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

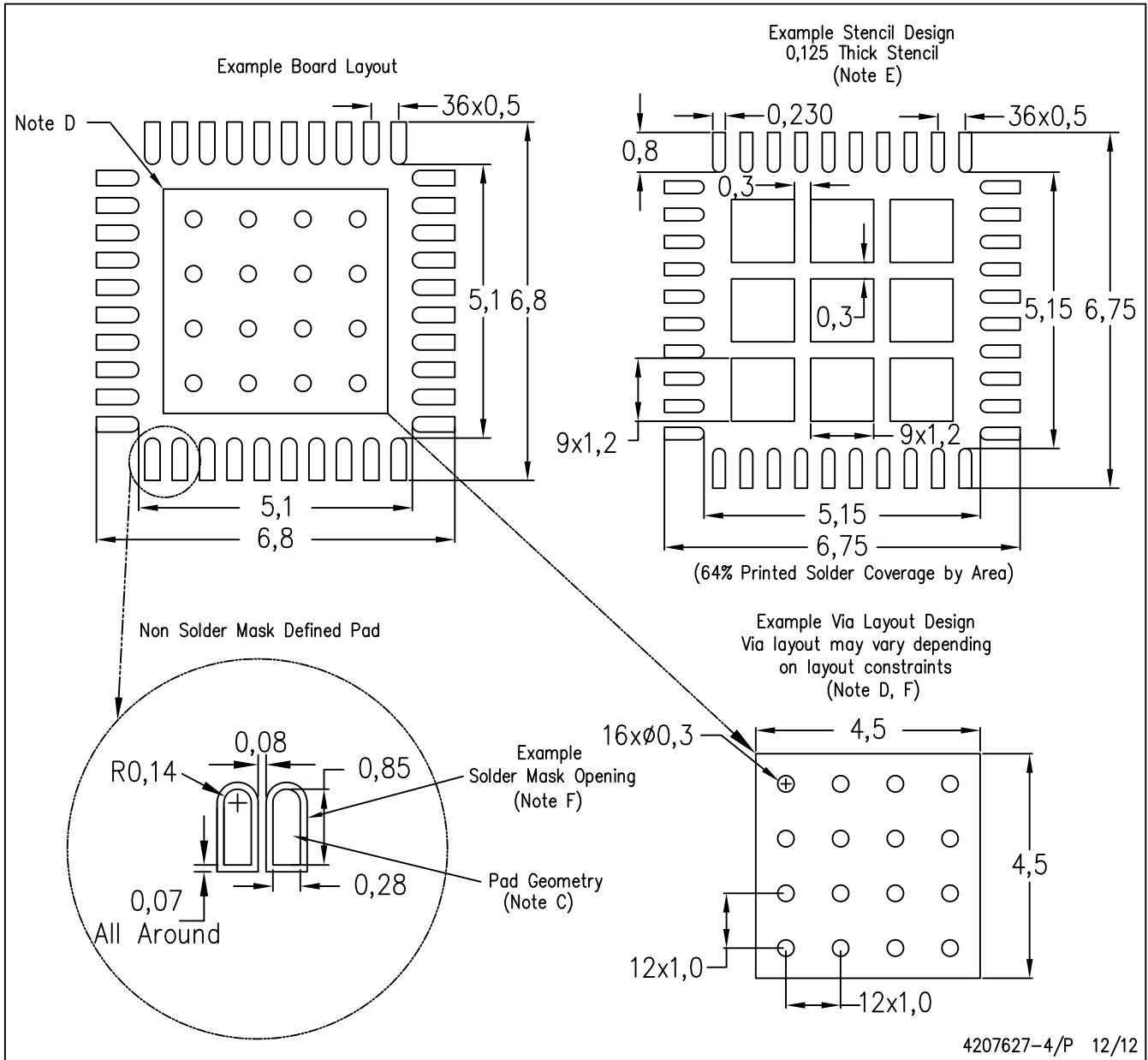
Exposed Thermal Pad Dimensions

4206355-4/U 12/12

NOTES: A. All linear dimensions are in millimeters

RHA (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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